Modeling of total dose radiation effect of RF PD SOI-MOSFET using Sentaurus TCAD

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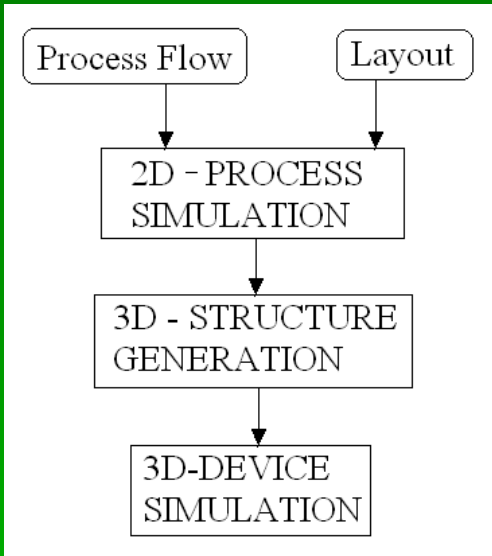
Advantages of partially depleted SOI – FETs versus bulk devices

- lower drain and source capacitances and high performance for digital and RF-applications
- full dielectric insulation of each transistor, low leakage currents, even at high operating temperatures, no latch-up in CMOS structures
- smaller layout dimensions
- higher immunity to total dose radiation and single event upsets (SEU)

Main targets of this article

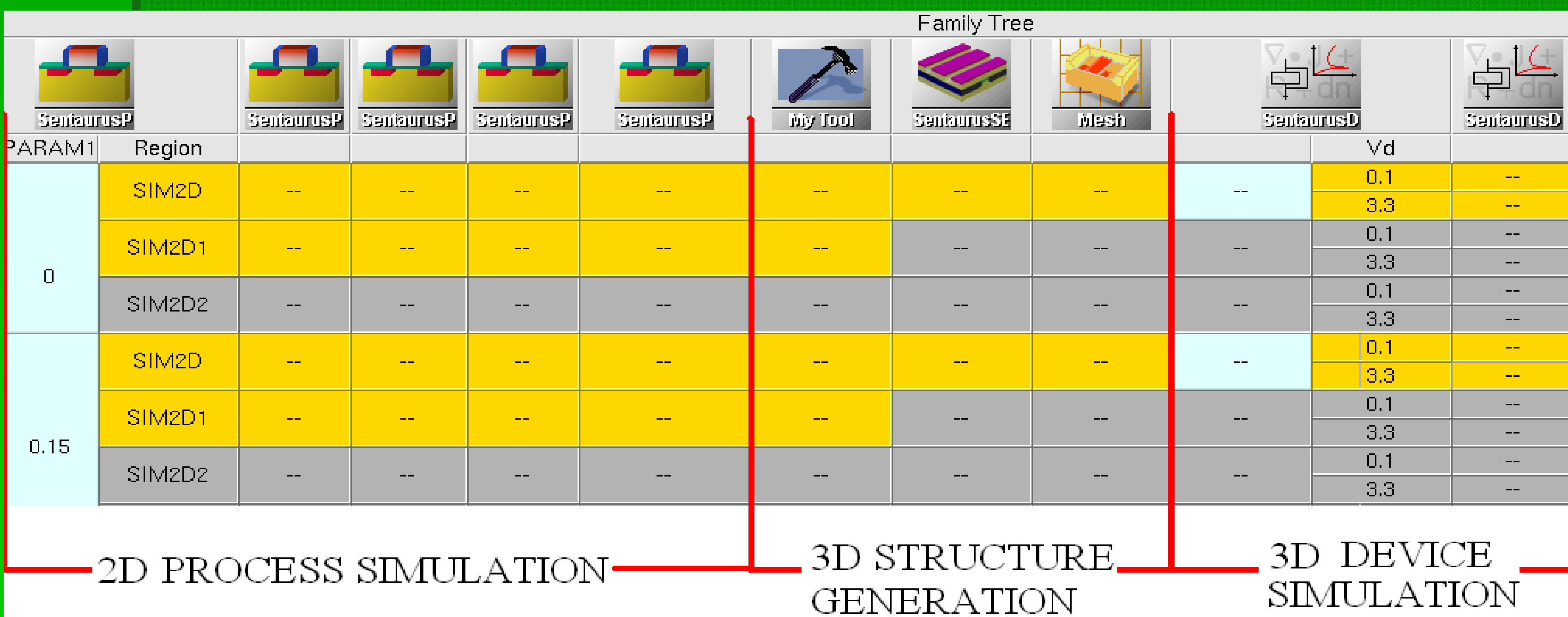
- perform 2D simulation of basic process flow and create 3D A-type SOI - device structure with different channel lengths (0.35 and 0.5 mkm) and widths: W=1,2,3 mkm
- perform DC-device simulation: simulate static current-voltage characteristics (Id(Ugs), Id(Uds))
- perform AC-device simulation: simulate small-signal dependences of H21(f) MUG(f)
- calculate dependences of f1(Ugs) and fmax(Ugs)
- calculate dependences of Id(Total Dose) using device simulation

Simulation flow



- Simplified simulation flow

- Total simulation flow in TCAD



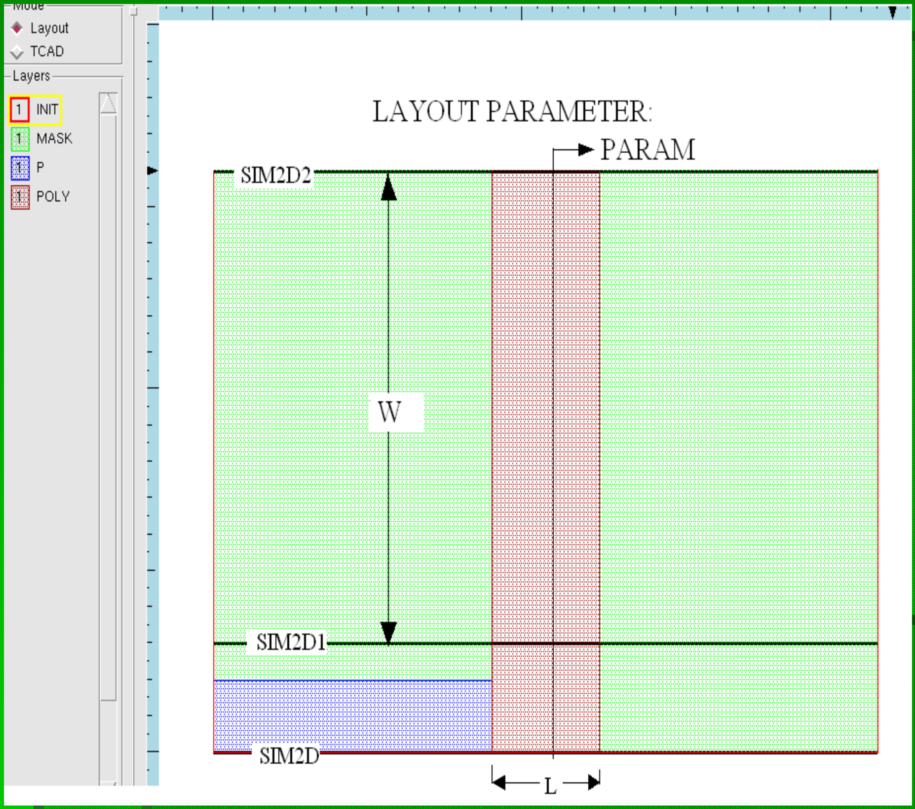
Family Tree

SentaurusP		SentaurusP	SentaurusP	SentaurusP	SentaurusP	My Tool	SentaurusSE	Mesh	SentaurusD		SentaurusD
PARAM1	Region									Vd	
0	SIM2D	--	--	--	--	--	--	--	--	0.1	--
										3.3	--
	SIM2D1	--	--	--	--	--	--	--	--	0.1	--
										3.3	--
	SIM2D2	--	--	--	--	--	--	--	--	0.1	--
										3.3	--
0.15	SIM2D	--	--	--	--	--	--	--	--	0.1	--
										3.3	--
	SIM2D1	--	--	--	--	--	--	--	--	0.1	--
										3.3	--
	SIM2D2	--	--	--	--	--	--	--	--	0.1	--
										3.3	--

2D PROCESS SIMULATION | 3D STRUCTURE GENERATION | 3D DEVICE SIMULATION

2D Process simulation

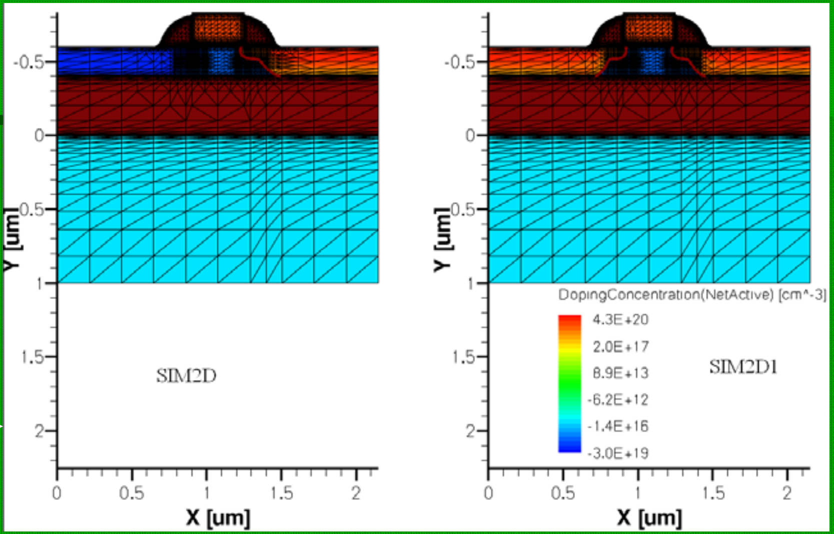
A-type transistor layout



Part of the total process flow

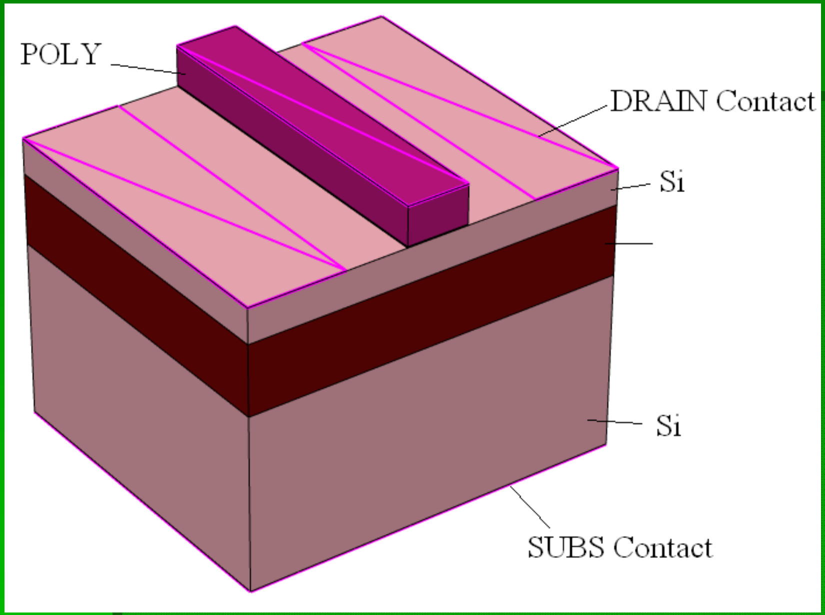
Variables & Macros | Flow | Unfolded Flow

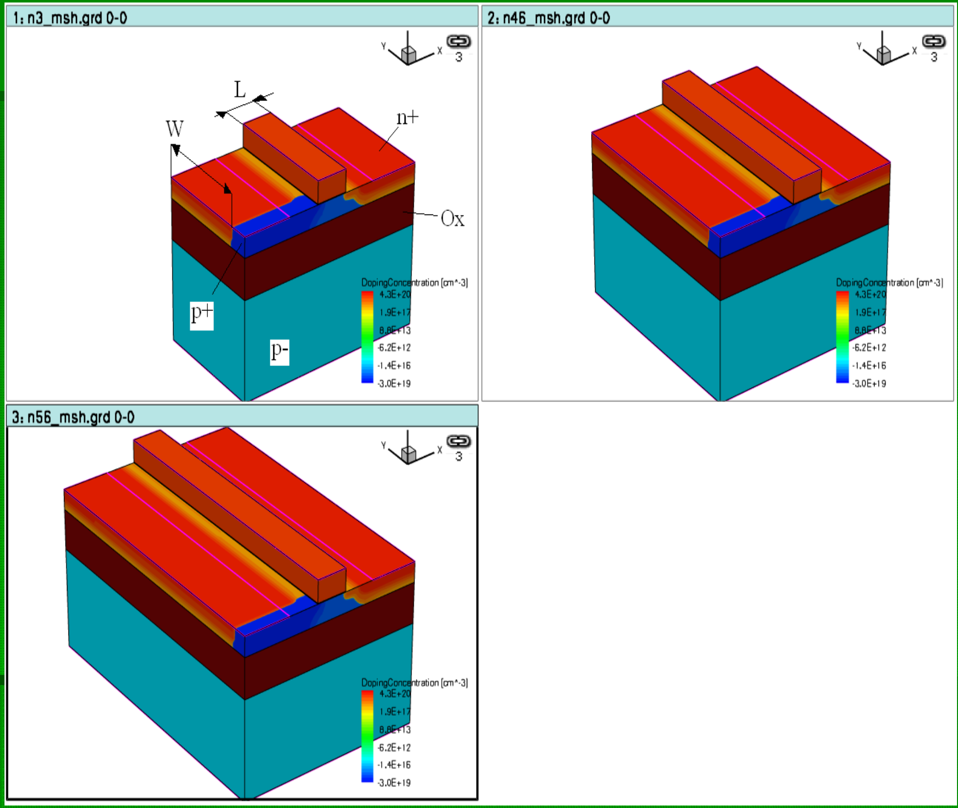
Names	Arg	Value	Arg	Value	Arg	Value	Arg	Value
Flow								
environment	title	An	save	true	grid	true	debug	false
SOI								
substrate	dopant	boron	concentration	1e15 /cm3	resistivity	12 ohm-cm	orientation	100
comment	text	NMOS						
insert	dios		sprocess	mgoals on	sde		tsuprem4	
deposit	material	oxide	thickness	400 nm	dopant	default	concentration	default
deposit	material	silicon	thickness	200 nm	dopant	boron	concentration	1e15 /cm3
active								
anneal	time	5 min	temperature	850 degC	pressure	1 atm	nitrogen	0 l/min
deposit	material	nitride	thickness	0.15 um	dopant	default	concentration	default
pattern	layer	ACTIV	polarity	light_field	thickness	1 um	side	front
etch	material	nitride	thickness	0.15 um	etch_type	anisotropic	overetch	10
etch	material	oxide	thickness	default	etch_type	anisotropic	overetch	10
etch	material	silicon	thickness	200 nm	etch_type	anisotropic	overetch	10
etch	material	resist	thickness	1.0 um	etch_type	strip	overetch	0
deposit	material	oxide	thickness	30 nm	dopant	default	concentration	default
STI								
deposit	material	oxide	thickness	0.4 um	dopant	default	concentration	default
etch	material	oxide	thickness	default	etch_type	specific	overetch	10
etch	material	nitride	thickness	150 nm	etch_type	isotropic	overetch	10
save	basename	An_STI_n@node@	format	grid	dios		sprocess	



2D process simulation of layout cuts SIM2D и SIM2D1

3D structure generation



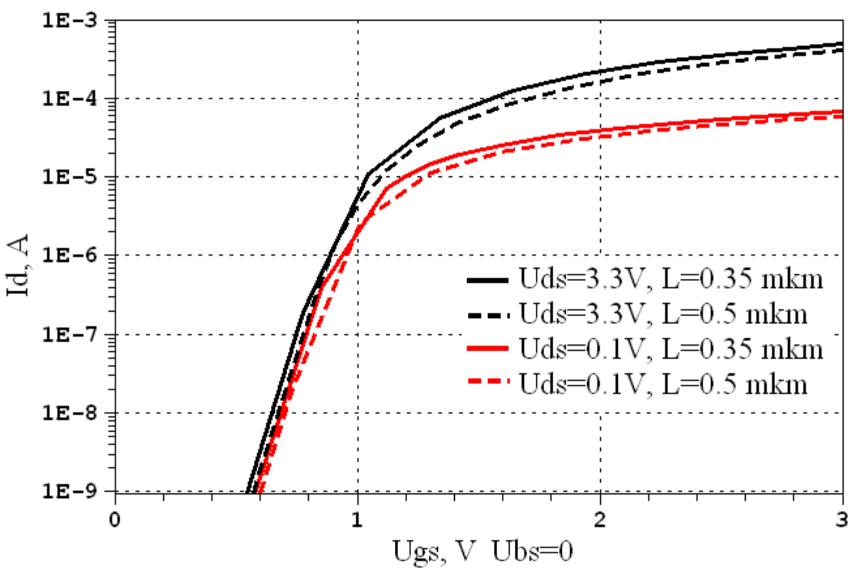


- 3D-device boundary

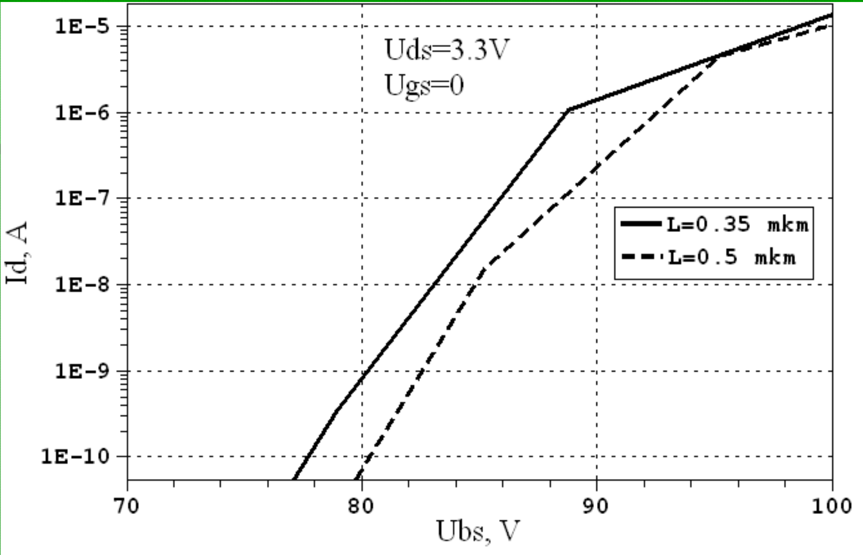
Final 3D-structures of A-type SOI-MOSFETS with W=1, 2, 3 mkm

Basic DC-simulation results

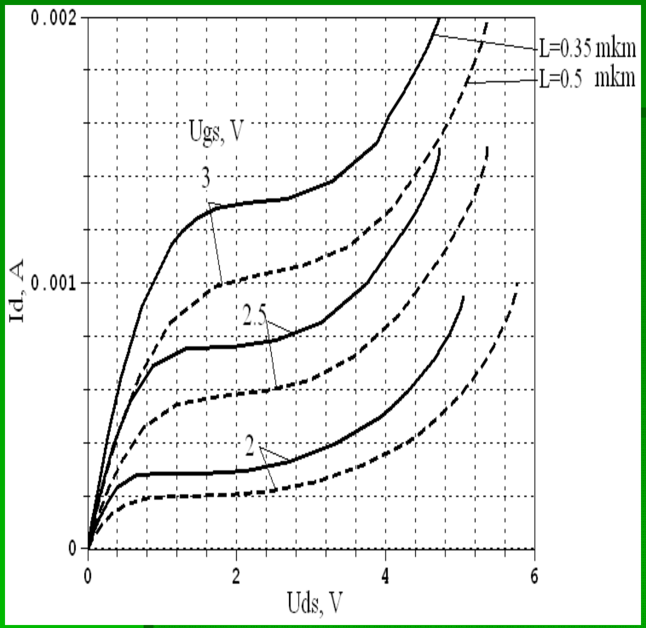
- Front Gate: Id(Ugs)
  Ut=1V



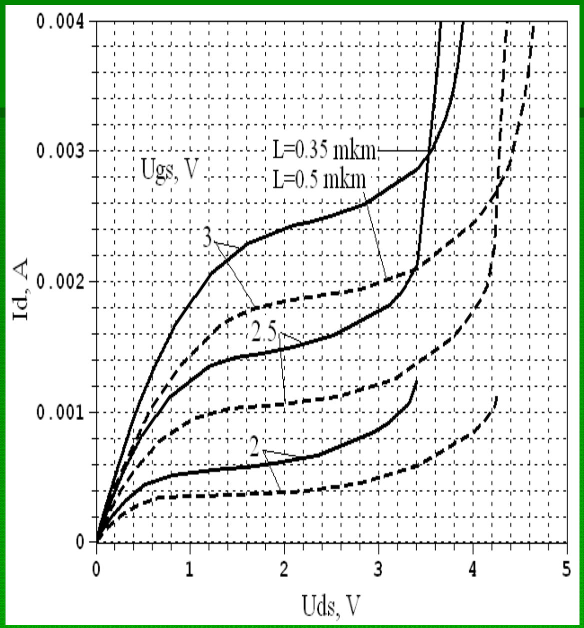
- BackGate: Id(Ubs)
  Ut=90 V



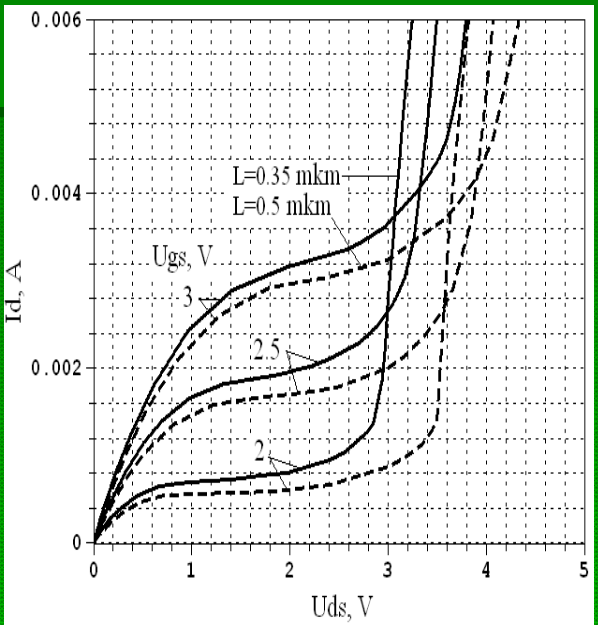
Simulated output DC- characteristics



W=1 mkm



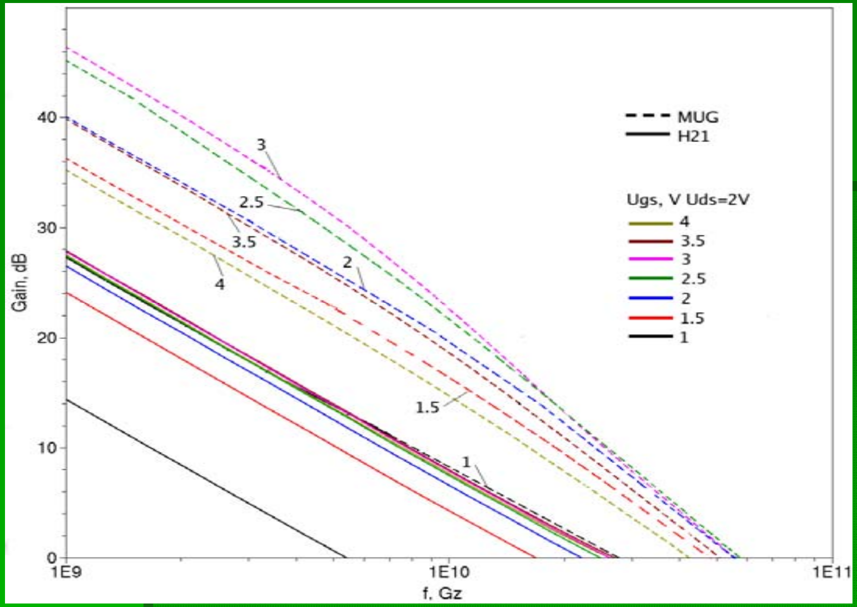
W=2 mkm



W=3 mkm

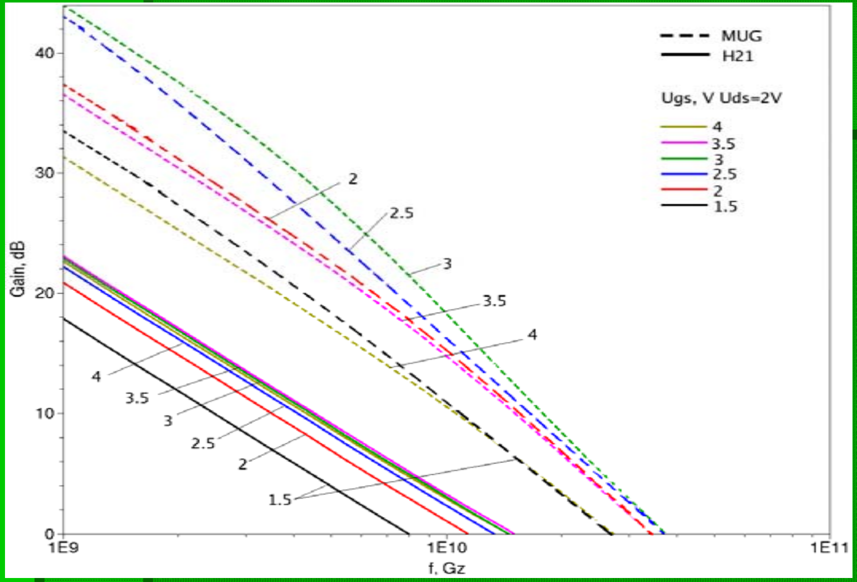
- Operating points for AC-analysis:
- Uds=2V, Ugs= 1- 4V

Results of AC-frequency analysis



- H21(f), MUG(f) for transistors with L=0.35 mkm

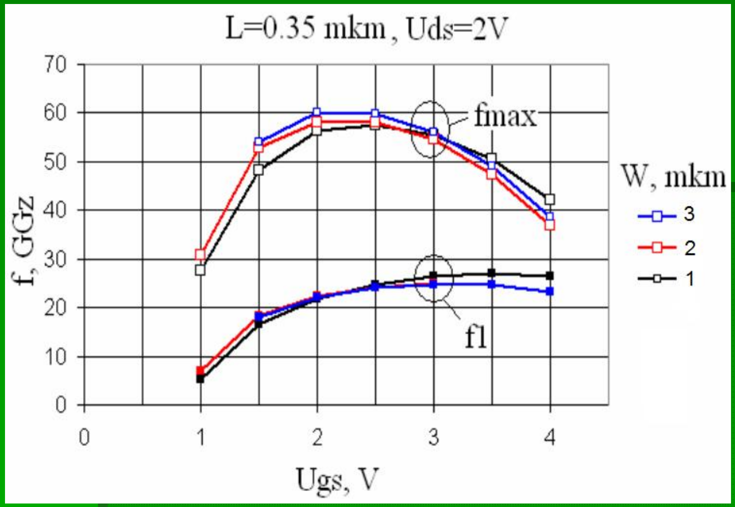
  and W=1,2,3 mkm

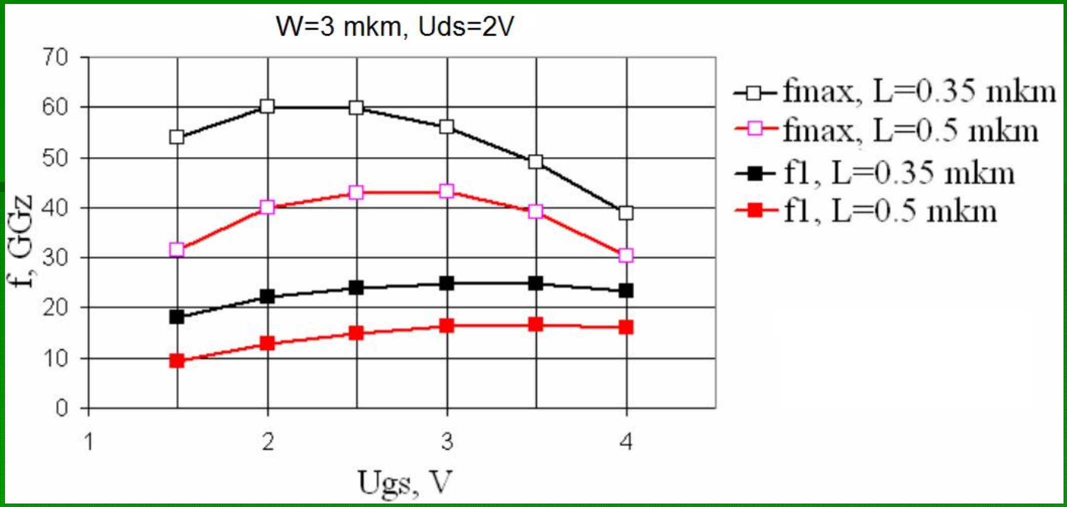


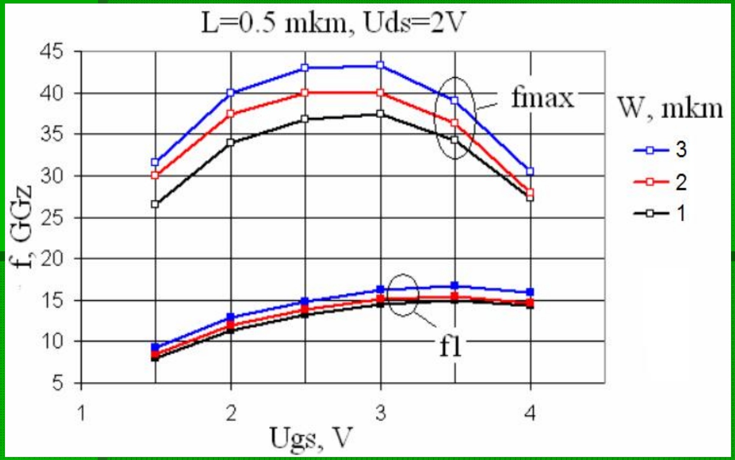
- H21(f), MUG(f) for transistors with L=0.5 mkm

  and W=1,2,3 mkm

Analysis of AC-simulation results







Dependences:

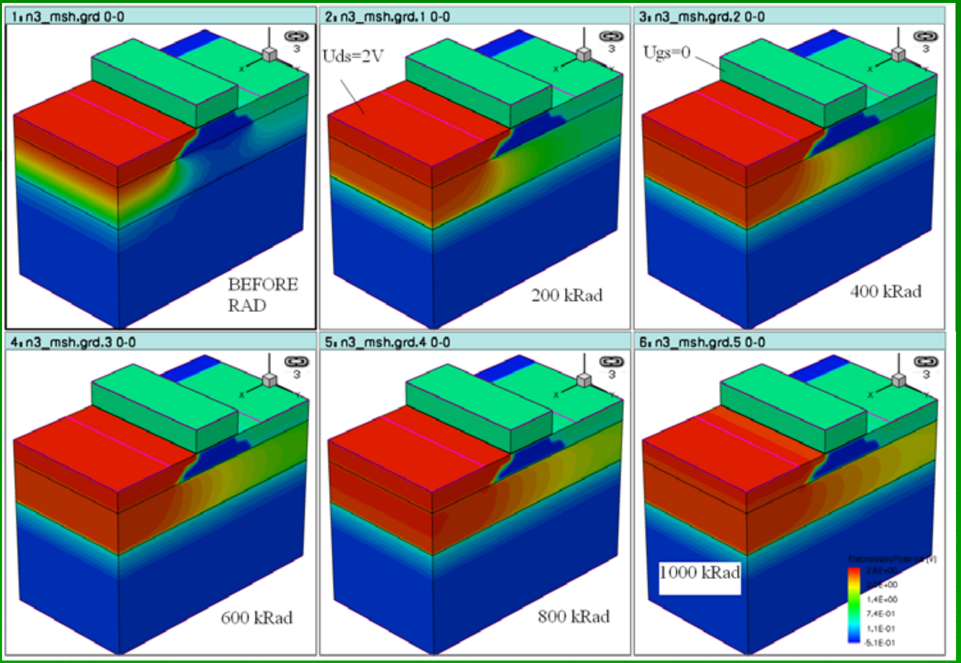
- f1(Ugs,L,W)
- fmax(Ugs, L,W)

L=0.35 mkm, Ugs=3V, Uds=2V: **f1 = 24 GGz, fmax = 57 GGz**

L=0.5 mkm, Ugs=3V, Uds=2V: **f1 = 17 GGz, fmax = 43 GGz**

Simulation of total dose effects

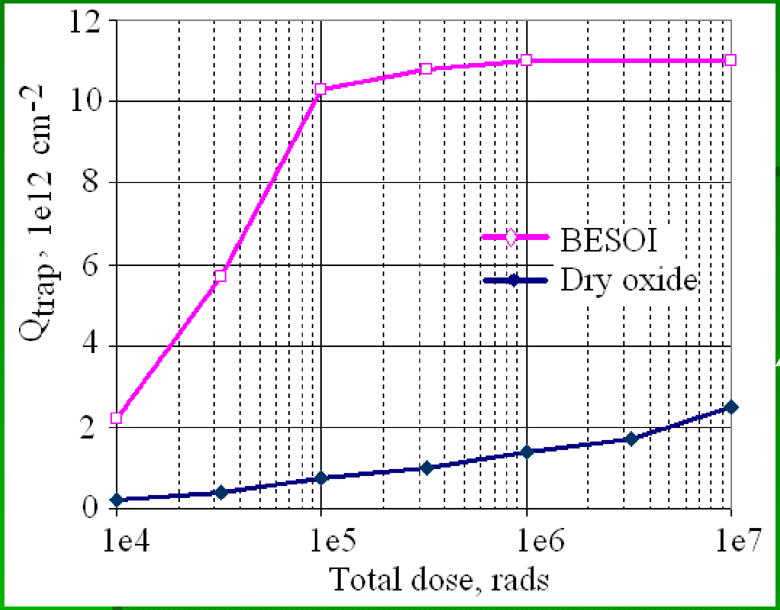
- Positive charge trapping occurs in oxides of SOI-structure, changing the potential distribution



- Define maximum concentration of neutral traps in oxide (Ctrap). This value strongly depends on oxide fabrication conditions

Potential distribution in A-type SOI-MOSFET before and during radiation. Uds=2V Ugs=0

Publications about charge trapping in oxides during irradiation



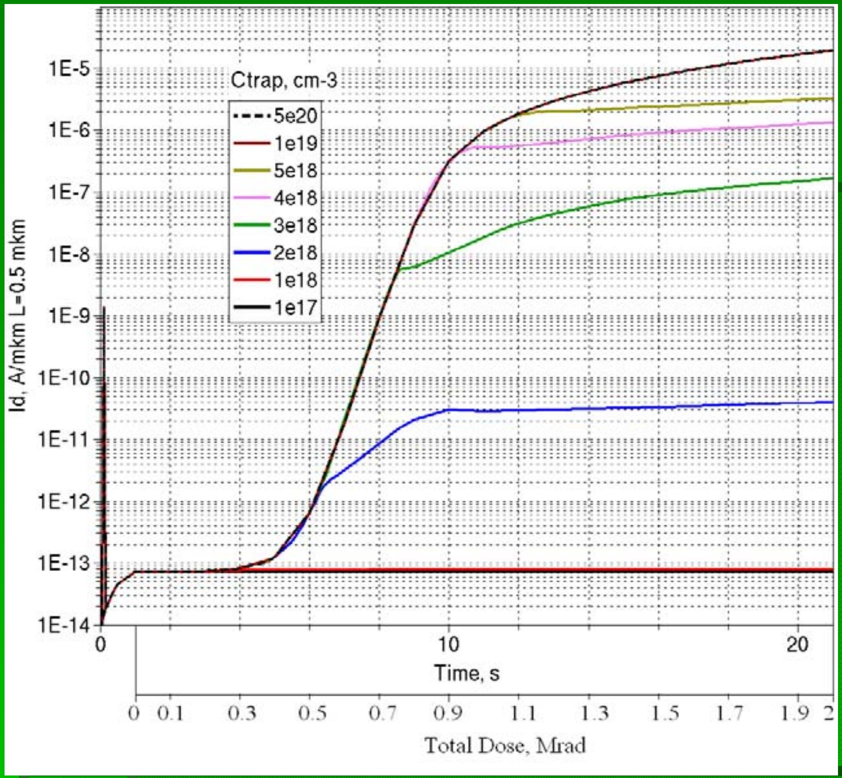
R.K. Lawrence et. al, "Positive charge trapping in SOI materials",
Proc. IEEE Intern. SOI Conf., 1996, p.34

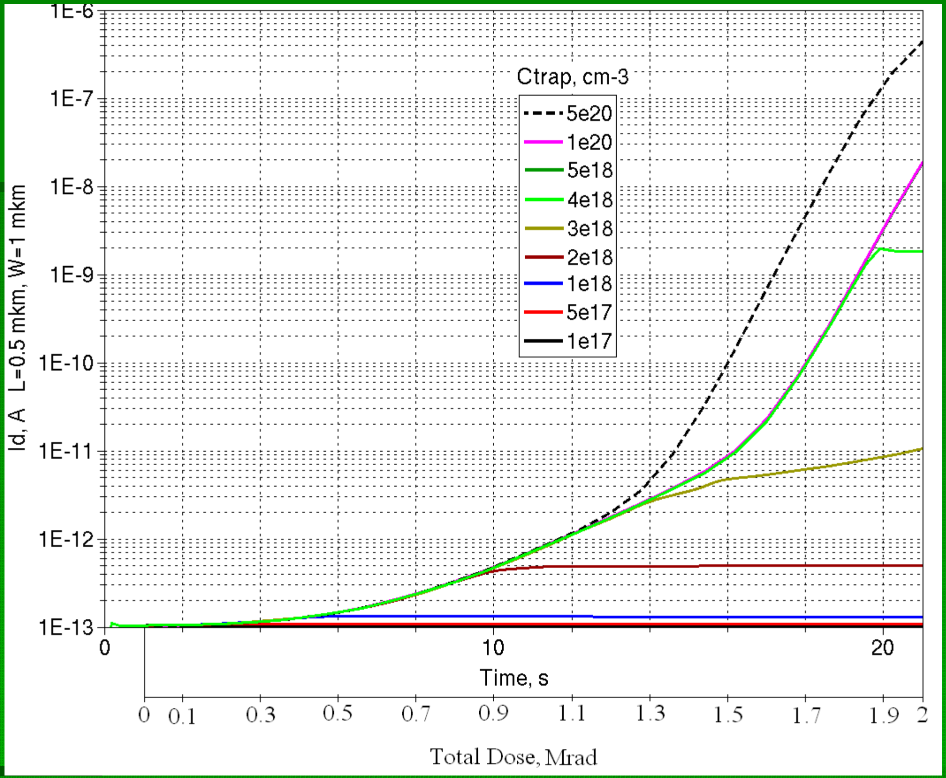
Dependence of surface trapped charge density versus total dose in different oxides Qtrap(Dose)

Dependence of bulk trapped charge density versus total dose Ctrap(Dose) in BESOI with Dox=400 nm

Ctrap=Qtrap/Dox

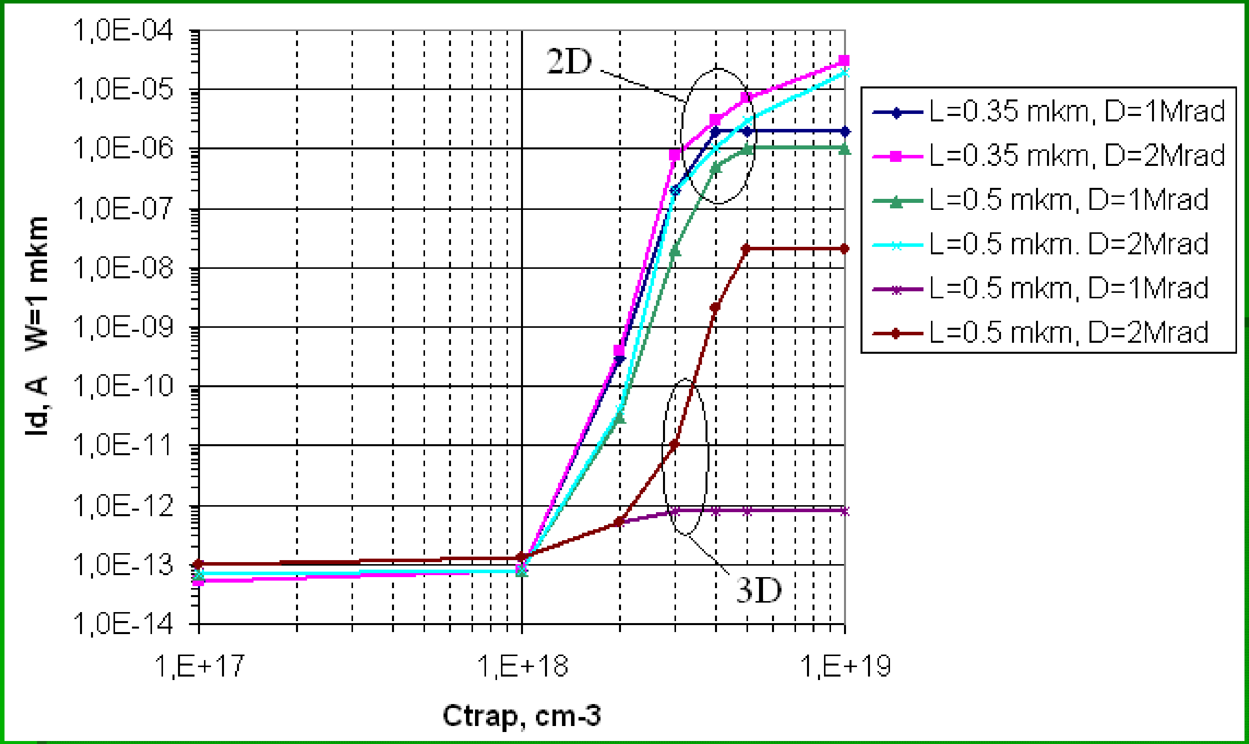
Results of total dose effect simulation





No body contact (2D) With body contact, W=1mkm (3D)

- Dependences of drain leakage current versus total dose
- Uds=2V, L=0.5 mkm, DoseRate=100 krad/s
- Ctrap – parameter: 1e17 – 5e20 cm-3



Dependences of drain leakage current versus maximum oxide traps concentration for different transistors at 1 and 2 Mrads

Qtrap=2.75e17 cm^{-3} <Ctrap=1e18 cm^{-3}

all our transistors, even without body contact – are radiation hard

Thank You!