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## CMOS Model's FLAG Control System

Overview: evolution of CMOS transistors models, Results of CMOS transistors models evolution, Drawbacks of existing approaches, Proposed approaches for model speed and accuracy increase, Target function definition for CMOS model speed and accuracy increase, Proposed flow for model speed and accuracy increase, Accuracy and speed increase flow application results, CMOS model speed and accuracy increase software structure and functionality, FLAG software graphical interface, FLAG efficiency estimation.

The first models (**slide 3**) of CMOS technology are very simple, which contains few differential equations and parameters. One of this models is BSIM1 in which $V_{th}$ is calculated with help of simple equation.

During transistor models evolution (**slide 4**) the models became more and more complicated: the accuracy of this models is higher than in BSIM1, but modeling time is increased. On the slide the example of $V_{th}$ parameter calculation with BSIM4 modle is presented.

Here (**slide 5**) the new physical effects that needed to be calculated in a technologies such as 45nm and 65nm and their equations are shown.

It mean that during COMS models evolution modeling became more complicated (**slide 6**), which comes from complications of equations and parameter number growth. For example simulation time of one transistor in BSIM4 is 1,5-2 times larger than in BSIM1, and for inventor it is larger by up to 2, 5 times.

The approaches is proposed for model speed and accuracy increase, for which the trade-off between number of operations and achieved accuracy is needed to find in every computational case (**slide 7)**.

Elimination of information lack and excess during calculations (**slide 8, 9**): BSIM4.4.0 models calculation situation is presented.

Transistor model computation flow (**slide 10**). Flag control in BSIM4 model is presented:

Trees of computational gates for exception of information lack and excesses (**slide 11**) are presented:

Different accuracy for transient simulation depending on demands occurring during current computational situation (Hierarchy of adaptation criteria used in CMOS transistor's model) (**slide 12**), Model versatiality: independency from modeling circuit type, technological

process, elemnt base, etc.; CMOS transistor compatibility with other electrical elements' models (diodes, resistors, etc): No need in recalculations during modeling with this models.

Proposed flow for model speed and accuracy increase (**slide 13**) 1. Technological information, simulation condition and specification input 2. Definition of CMOS model and number of models in hierarchy of equations 3. Designed IC preliminary and fast simulation with low accuracy 4. Simulation results for designed IC meet specification 5. Definition of model flags for designed and reference circuit 6. Designed and reference circuit description formation 7. Simulation of reference circuit 8. Simulation results for reference IC meet specification 9. Simulation of designed IC.

The example of low to high level shifter's accuracy and speed increase is shown (**slide 14**).

In this step (**slide 15**) low accuracy and fast simulation is performed with help of LEVEL4 models.

Frequency simulation results for gate's capacitive and tunneling currents and time dependence from number of computational gates for TSMC65 (**slide 16**) presented. On these results the values for flags will be defined.

For this case the gain in accuracy is 99,78% and in modeling time is 57,14s. (**slide 17**).

With help of abov mentioned algoritm FLAG software created for model speed and accuracy increase (**slide 18**).

Example shows two working windows for IC simulation parameter selection and Input of model different parameters is shown(**slide 19**).

There comparative results with most famous software with FLAG are shown (**slide 20, 21**) for efficiency estimation.

1 SYNOPSYS

2 CADENCE