Development and research of IP-blocks verification method by Perl language

What is the system on a chip?

"System on a chip" (SoC) it is not just difficult special ASIC. SoC essentially differs from traditional ASIC (Application Specific Integrated Circuit) both structure, and designing methodology. In drawing 1 the example classical **"systems on a printed circuit board (PCB)"** is presented. Such system gathers from finished electronic components: special ASIC, semicustom IC, IC average and small degree of integration, and also discrete elements (transistors, resistors), etc.

System-on-a-chip refers to integrating all components of a computer or other electronic system into a single integrated circuit (chip). It may contain digital, analog, mixed-signal, and often radio-frequency functions – all on one chip. A typical application is in the area of embedded systems.
The contrast with microcontroller is one of degree. Microcontrollers typically have under 100K of RAM (often only bytes), whereas the term SoC is typically used for processors capable of running software such as Windows or Linux.

The example "systems on a chip" is presented in drawing 2. At the heart of methodology of designing SoC lies the principle of reuse Intellectual Property of the blocks (IP-blocks) developed purposefully or within the limits of any project (lies?). By analogy to system on a printed circuit board (PCB) where as components finished microcircuits act, the system on a chip is designed from reusable blocks.

IP-blocks are, in point of fact, mathematical models (topology, the list of chains, a RTL-code) of functional-finished blocks and knots SoC. Basic feature of IP-blocks consists in possibility of their reuse in other projects SoC. It their name speaks - IP (Intellectual Property), it means object of intellectual property. As IP-blocks in a sense are analogues electronic component them often name VC - Virtual Component.

Creation process "systems on a chip" means the decision of following tasks:

1) Working out of IP-blocks;
2) Designing SoC at systemic-functional level from Virtual Component;
3) Integration of all blocks on a chip.

Examples of IP-blocks which are most often used in projects SoC are presented:

- Programmed devices (microprocessors): RISC, DSP;
- - Memory: RAM, DRAM, Flash;
- - Standard interfaces: PCI, USB, Ethernet, etc.
- - Video and audio decoders: MPEG2;
- - Digital-to-analog blocks: ADC, DAC;
- - Analog and Vch-components: PLL (Phase-Locked Loop).

Advantages "systems on a chip" before classical "systems on a printed circuit board" are:

1) **Miniaturization:** As a rule, the device created on the basis of SoC consists of one (a maximum 2) ASIC and the limited set discrete components which for the technological reasons cannot be integrated inside IC;
2) **Power consumption decrease:** ASIC type "system on a chip" are made on technology "deep submicron" (DSM - Deep Submicron) 0.35 microns and more low that allows to lower source voltage and, as consequence, it is essentially reduce power consumption.
3) **Reliability increase:** Combination several components (IP-blocks) on one silicon wafer allows to reduce essentially number brazed connections.

Application fields of "systems on a chip" are:

- Communication system and telecommunications, in particular, a wireless communication of standards GSM and WCDMA;
- - Information networks (LAN, the Internet), in particular, wireless networks of standard IEEE 802.11 (BlueTooth, Wi-Fi);
- - Digital television;
- - Radio navigation (GPS, Glonass);
- - Multimedia applications and household electronics.

Classification and IP-blocks design problems

IP-blocks are the valuable goods in the market of microelectronics and are classified on a method of licensing - volume of that information which is given by the developer of a core to the customer.

In total there are three approaches:

1) **“Soft core”** - The most expensive license as the customer receives initial texts in languages Verilog and VHDL with the description not abstract functionality, but the scheme, suitable for synthesis with using libraries of elements of the concrete manufacturer.
2) **“Firm core”** - the scheme optimized on library elements of the chosen manufacturer and ready for wiring layout is offered to the customer. The customer cannot restore an original function scheme, but is capable to repeat only circuit decision, at that in the license the quantity of admissible repetitions can make a reservation.
3) **“Hard core”** - the most hard variant when the sample of the geometry, a finished topological part, a library element is on sale. The owner of the licence lets out pilot lots of a licensed IP-core at different manufacturers. The part of a chip occupied with an IP-core is fixed, and costumer keep the rest part of the

chip for filling with the scheme and a set of ports for coupling interface to an IP-core. If the customer asks to move the IP-block to other place, the licence manages a bit more expensively because its holder any change of topology considers as the new project.

So, we have found out that application of IP-blocks (Intellectual Property - intellectual property) can be considered as a basis of modern long-term strategy of creation of new architecture.
Basic feature of IP-blocks is possibility of their reuse in other projects SoC.

IP-cores incorporation technologies in the general chip develop by research commands within 20 years. About seven years ago, during a time of creation of the first SoC, developers of componential cores (at that time having dimension by 2000-50 000 gates) have started development of the agreements providing their compatibility. The important questions which are discussed today, this licensing, development of standards on interconnections of IP-cores, system assemblage on a crystal from IP-cores. With a wide circulation of IP-cores "pure" semi-conductor architecture will cease to exist.

But there are some problems.
One of IP-blocks design problems is that reuse-block cost on the average in 10 times exceeds cost of the similar unitary used block, and for processors this size 10 times more. For this reason reuse-blocks are intended, as a rule, for the decision of general, logically formalizable problems, for example, the MPEG-coder, CPU, DSP, USB - and PCI - interfaces, etc. At a choice of IP-blocks cost of the finished block is considered and expenses for working out of the own are estimated.

However getting of a necessary set of IP-blocks is only the first step to the «system on a chip». Difficulties already begin at a combination stage in one project of gained and own IP-blocks. Besides differences in manufacturing techniques ASIC (that is anyhow considered in model), there are differences and methods of the description of the same models by different programmers.

To reduce such discrepancies to a minimum, suppliers and consumers of IP-blocks unite in association in which frameworks the major procedures are unified. The most known alliance is VSIA (Virtual Socket Interface Alliance) in which enter almost all known manufacturers of microcircuits and design centers which specializing on SoC.