
TIQ Based Analog to Digital Converters and Power Reduction Principles

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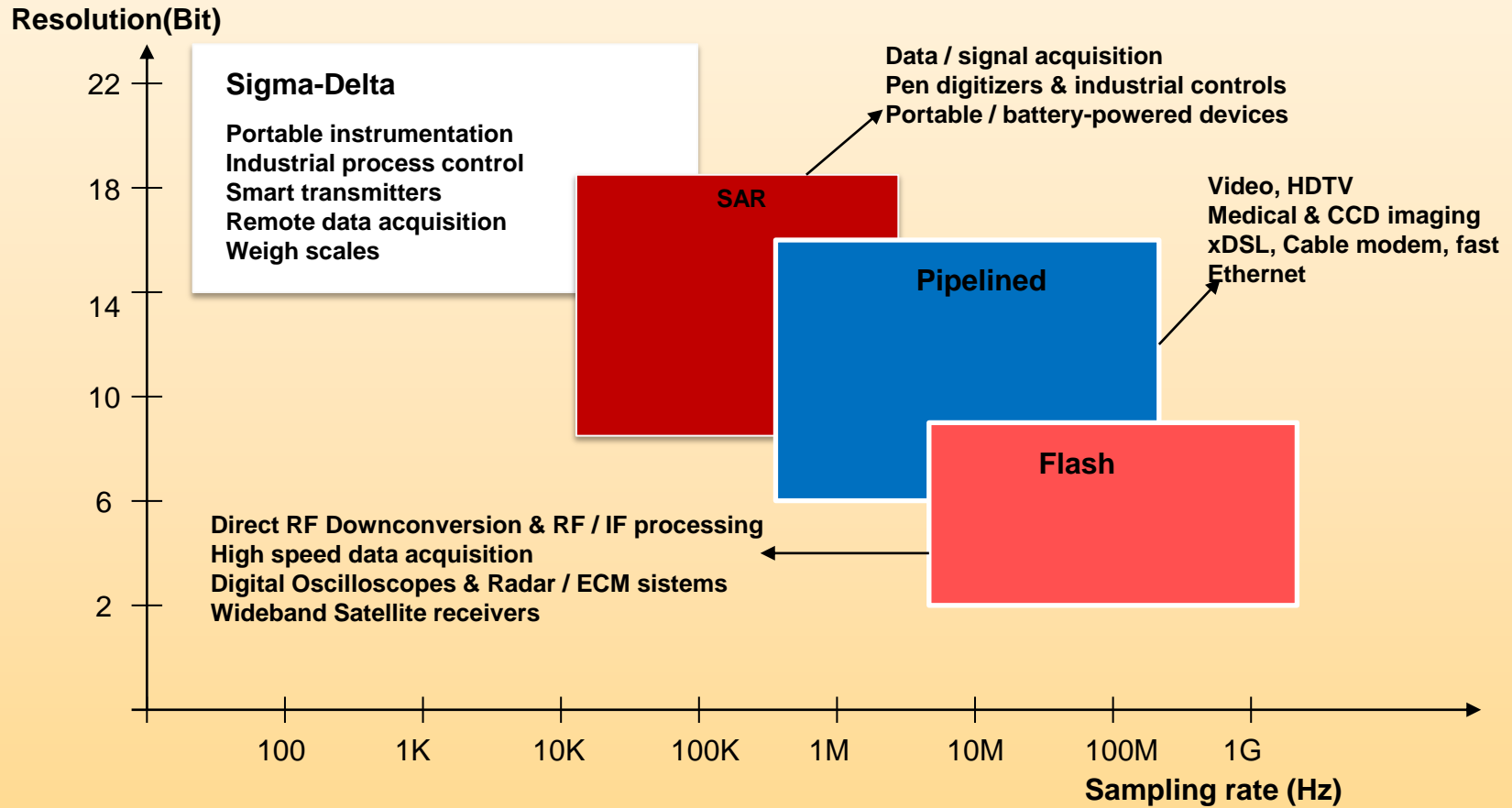
Moscow
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Outline

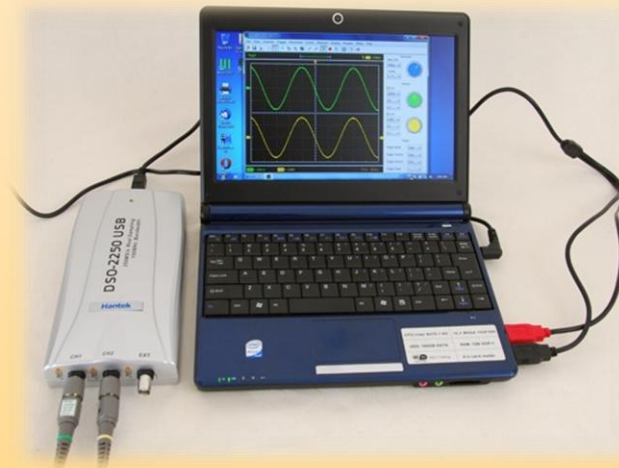
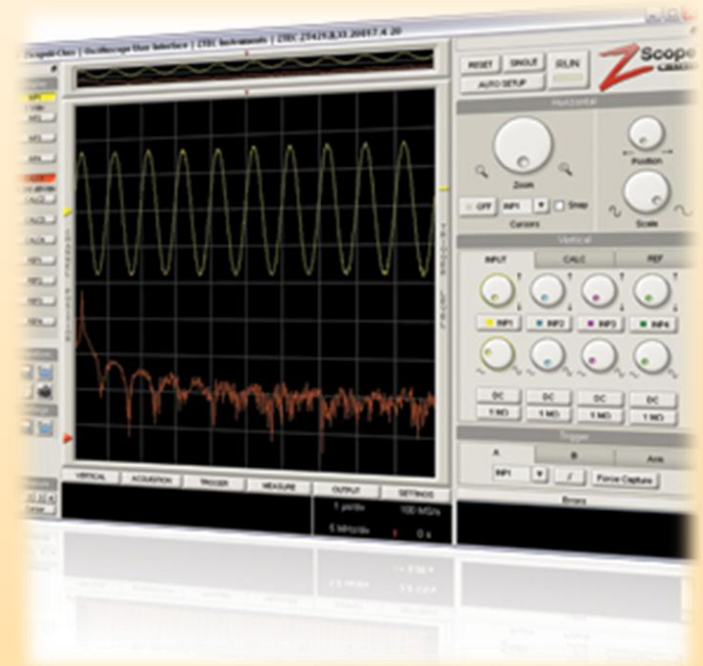
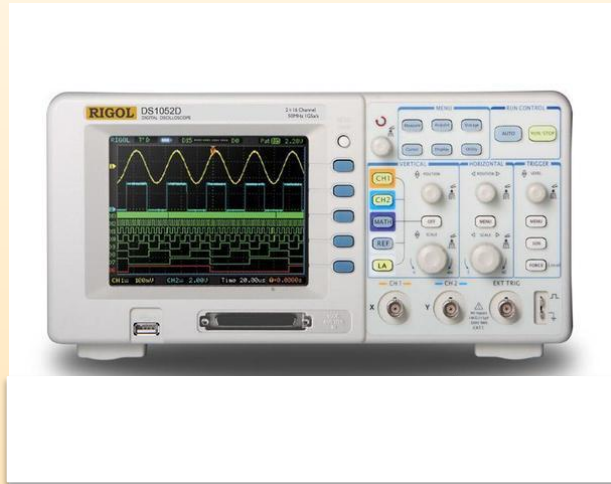
- **Trade of Between Resolutions and Sampling Rates**
- **Block Diagram of a Flash ADC**
- **TIQ Flash ADC**
- **CMOS Inverter as a Comparator**
- **Advantages and Disadvantages**
- **Quantum Voltage Comparator**
- **Power Management Method**
- **The Power and Resolution Adaptive ADC**
- **Conclusion**



The Power and Resolution Adaptive Flash ADC



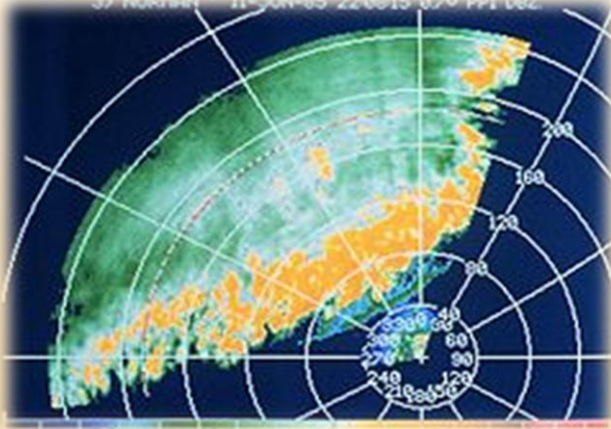
Applications: Digital Oscilloscopes



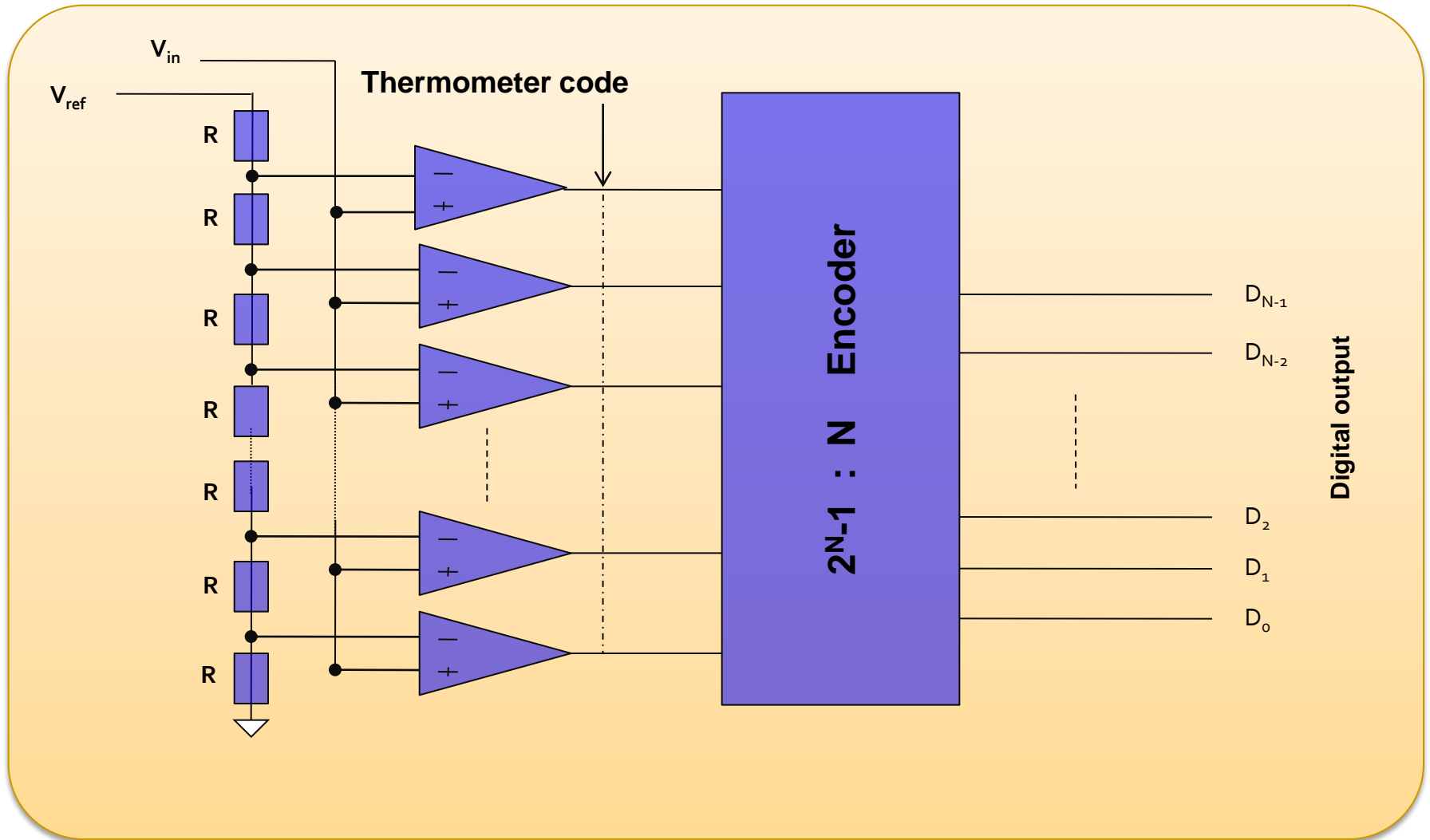
Applications: Satellite Receivers



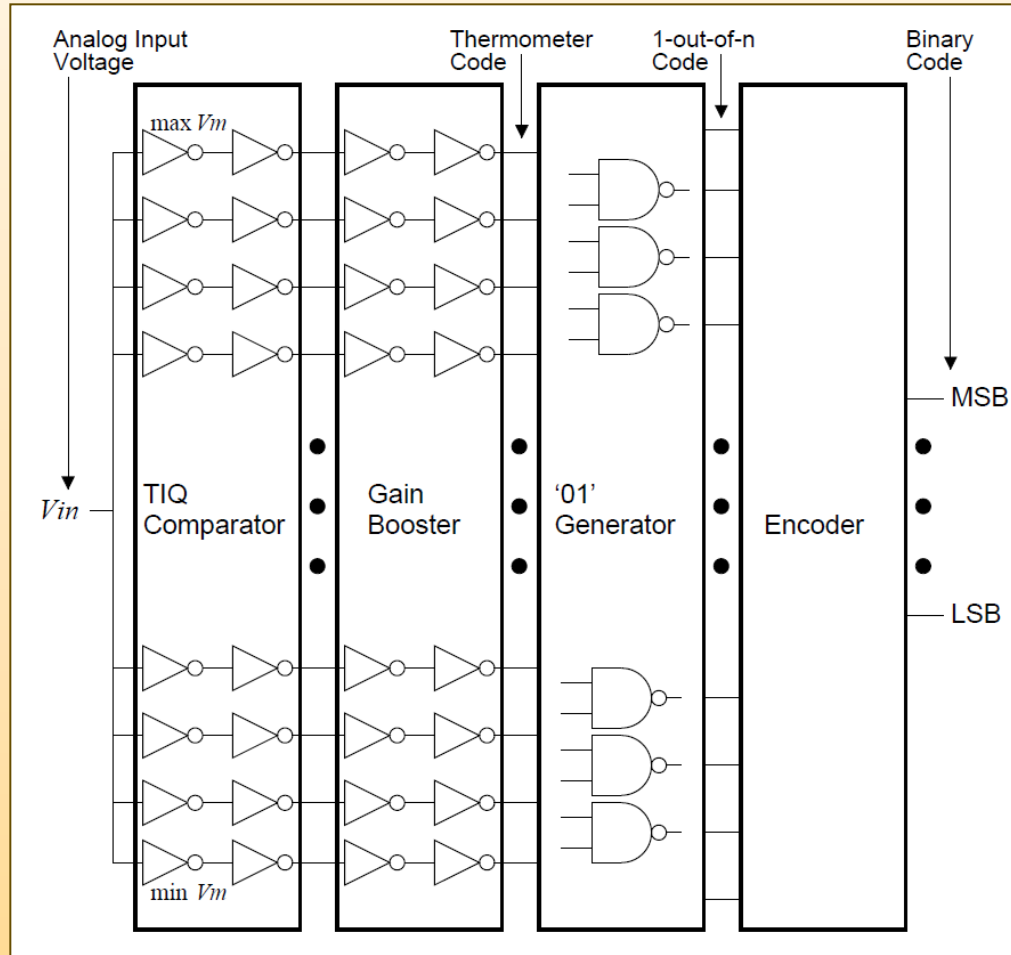
Applications: Radar Systems



Block Diagram of a Flash ADC



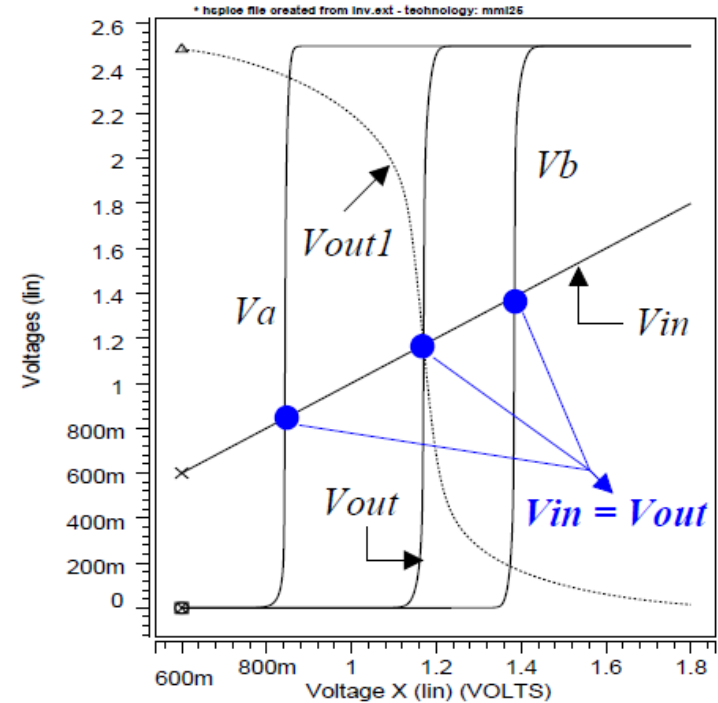
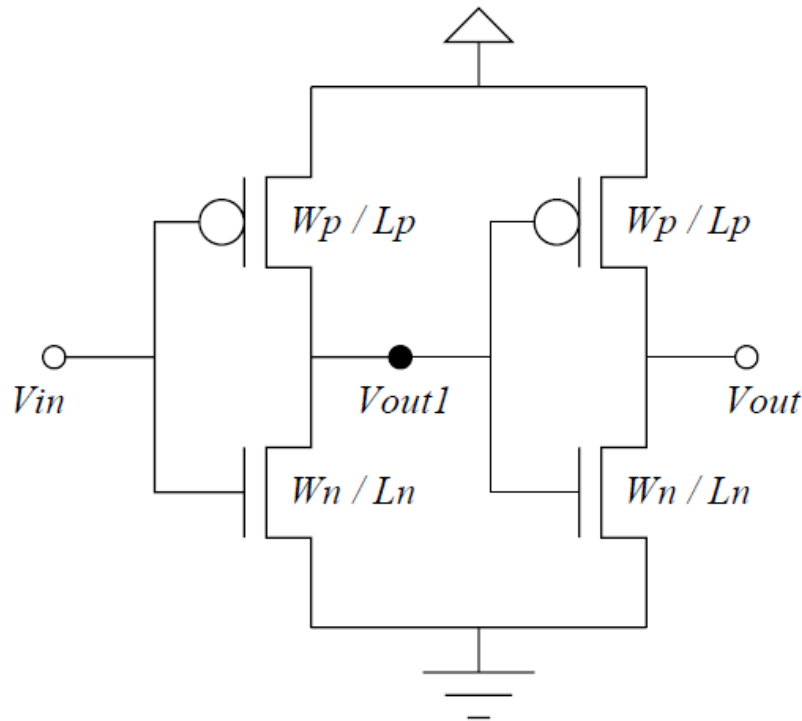
TIQ Flash ADC



TIQ

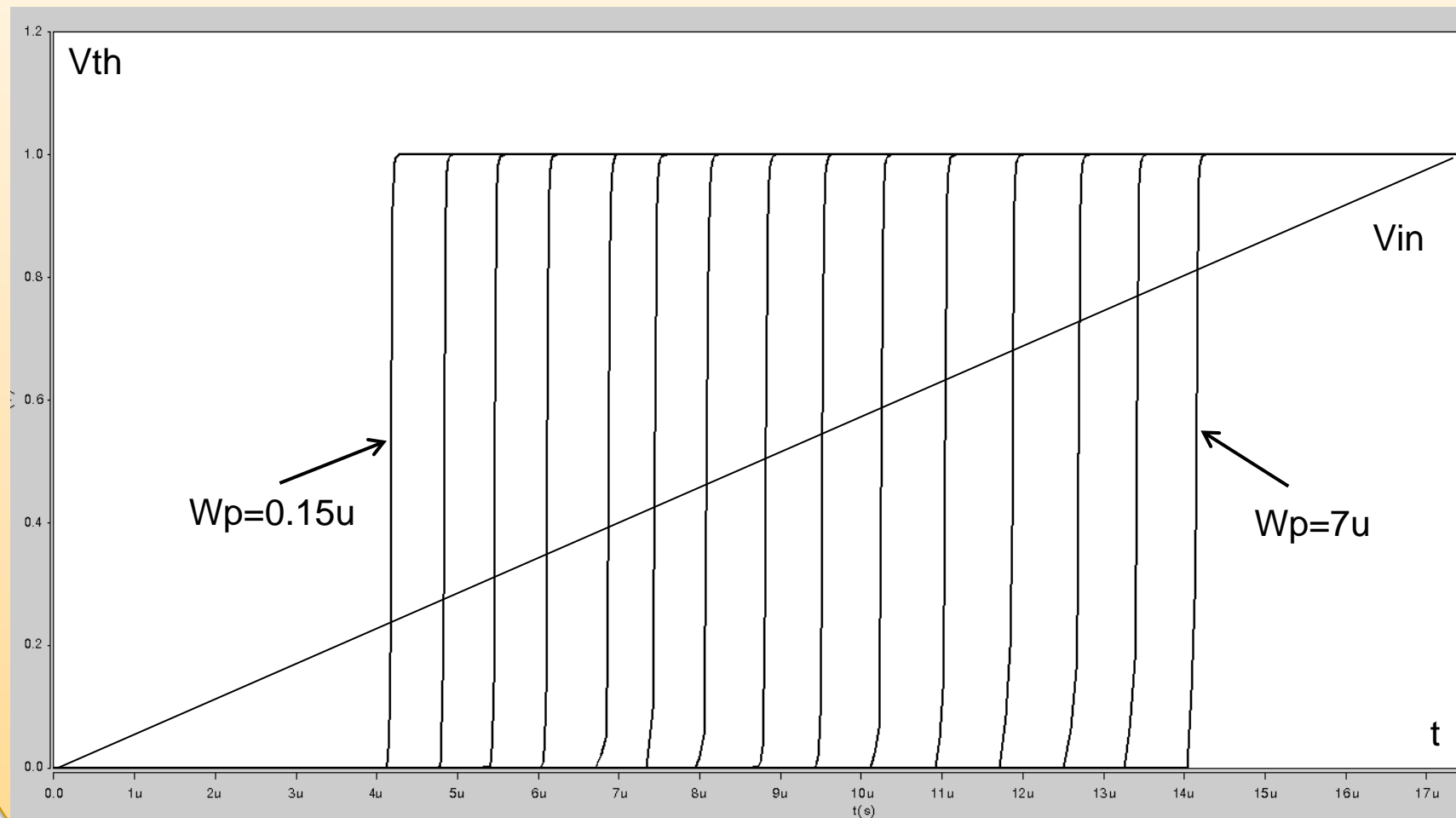
Threshold Inverter
Quantization

CMOS Inverter as a Comparator



$$V_m = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}} (V_{DD} - |V_{Tp}|) + V_{Tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}$$

Simulation Results for 4bit ADC



Comparator Sensitivity

Sensitivity to Temperature and Power Supply Voltage

$$\frac{\partial V_m}{\partial T} = \frac{1}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}} \left(\frac{dV_{Tn}}{dT} - \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}} d|V_{Tp}|}{dT} \right)$$

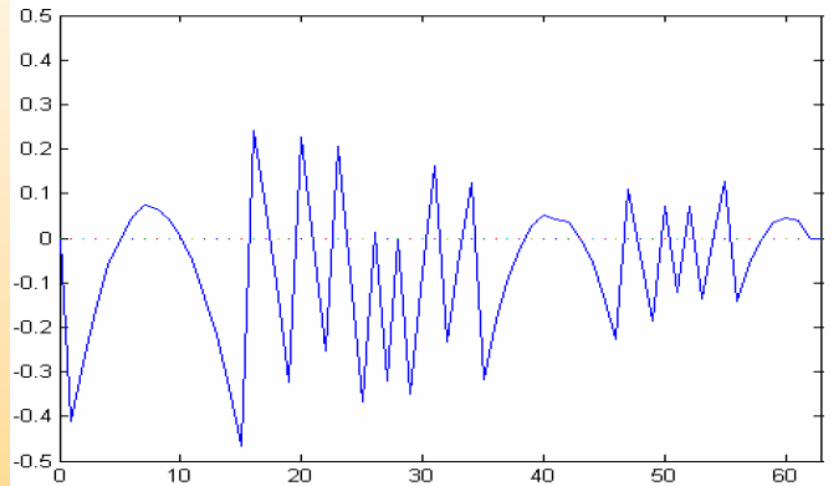
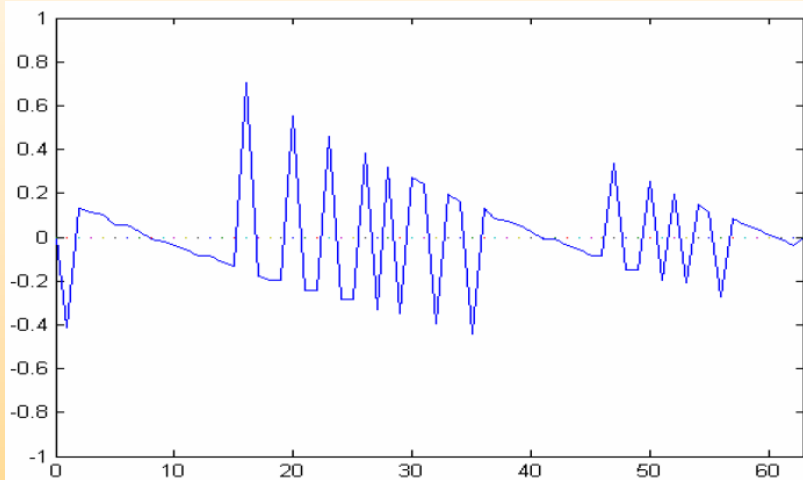
$$\frac{\partial V_m}{\partial V_{DD}} = \frac{1}{1 + \sqrt{\frac{\mu_n W_n}{\mu_p W_p}}}$$

Simulation Results for Comparator Sensitivity

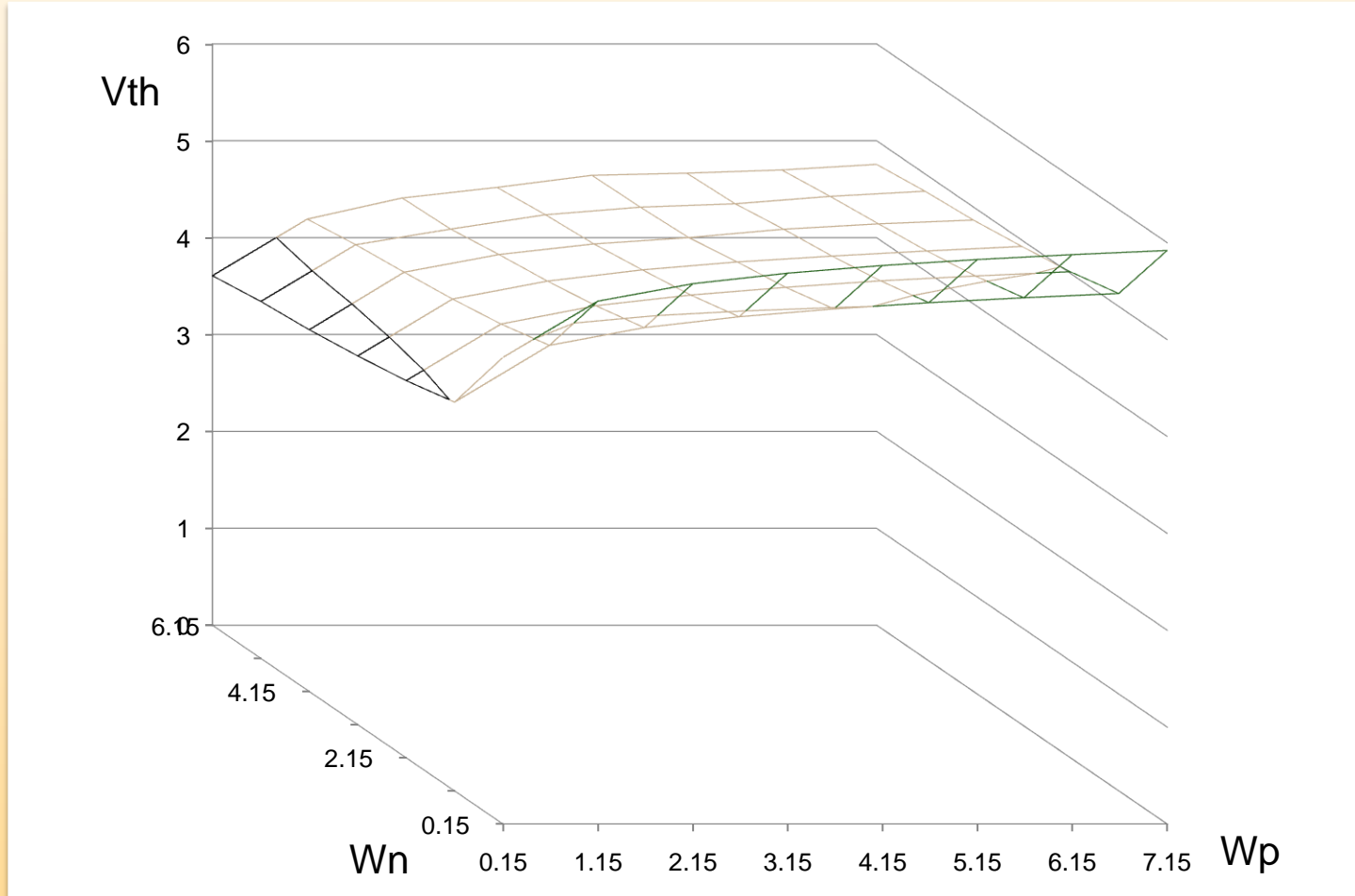
Variations	Min Vth (V)	Max Vth (V)
-40 C	0.42	0.65
25 C	0.43	0.67
125 C	0.44	0.68
1V (-5%)	0.4	0.6
1V (+5%)	0.47	0.66
Max deviation	3.1 %	6.5%

Integral and Differential Nonlinearity

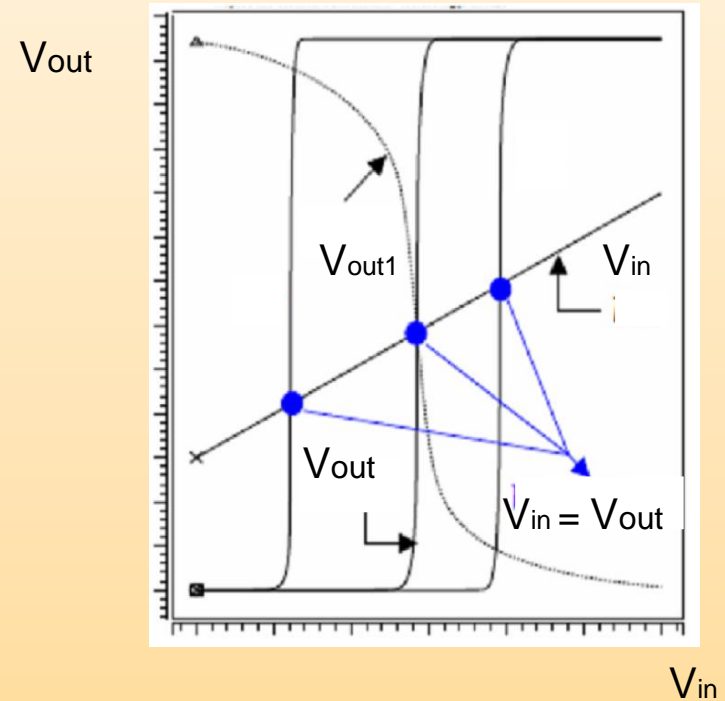
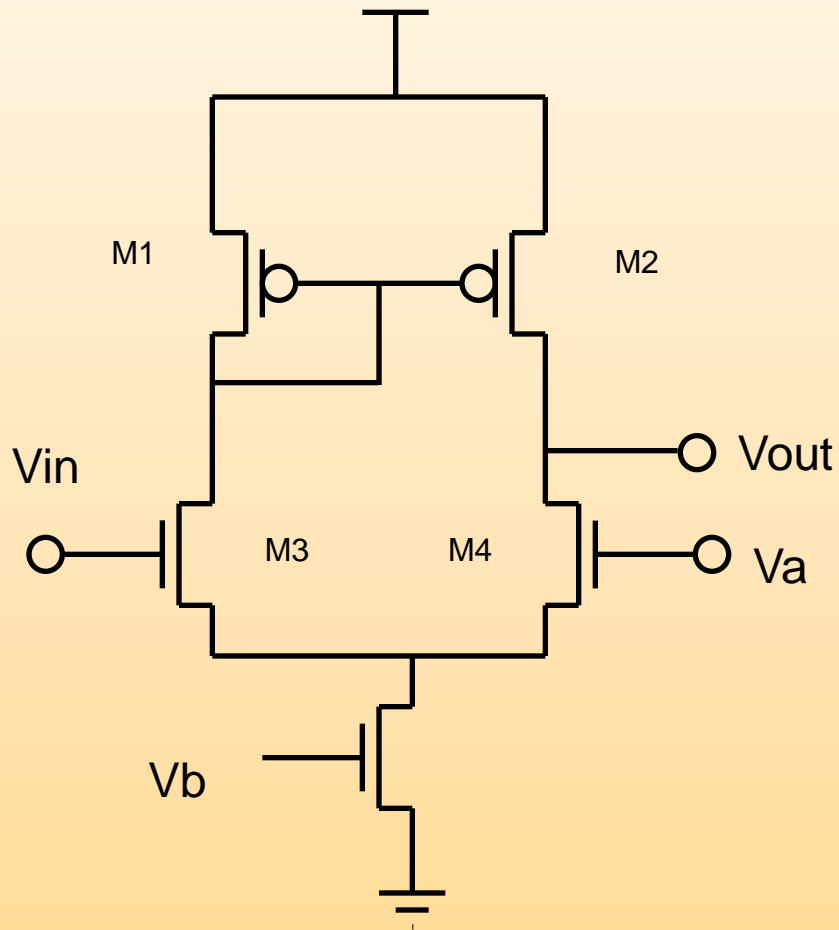
The internal voltage reference varies due to the process parameter variation during manufacturing. Such variations create limits on the linearity variation of the ADC



Systematic Size Variation Method



Quantum Voltage Comparator



Advantages

- Adaptable to future CMOS technology development, going to smaller feature size and lower supply voltage
- No need for a resistor ladder circuit as the reference voltage source
- No need for switches, clock signals, or coupling capacitors for the voltage comparison
- Suitable for the standard CMOS technology - ideal for the complete SoC implementation

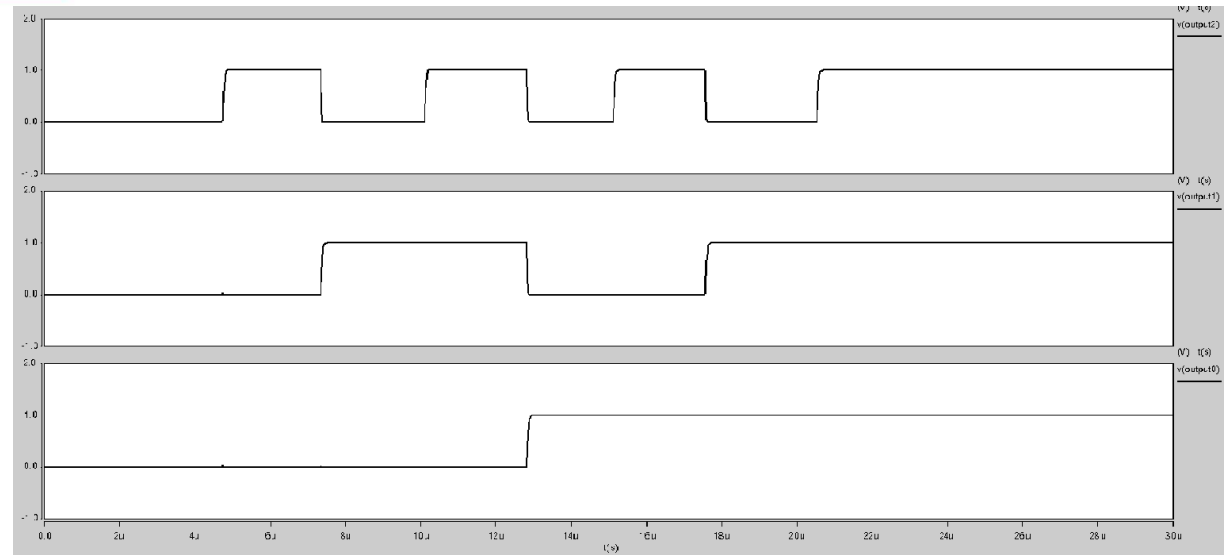
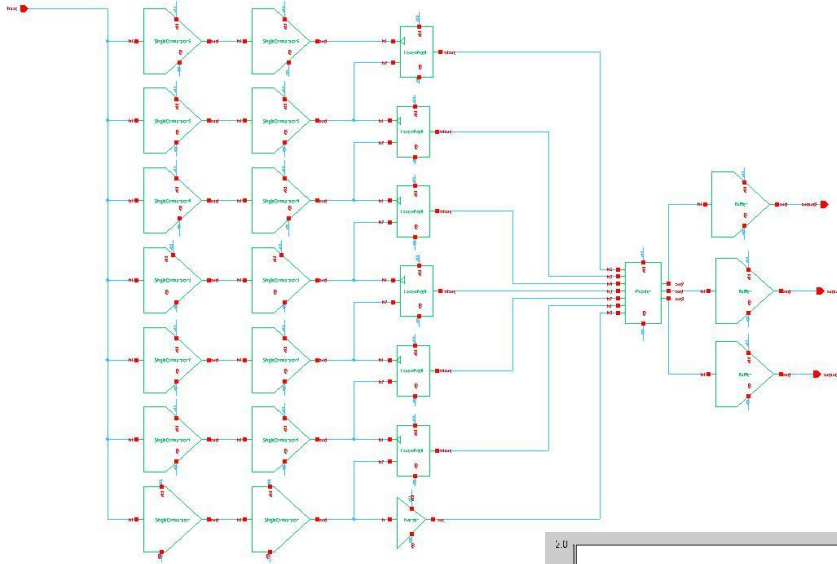


Disadvantages

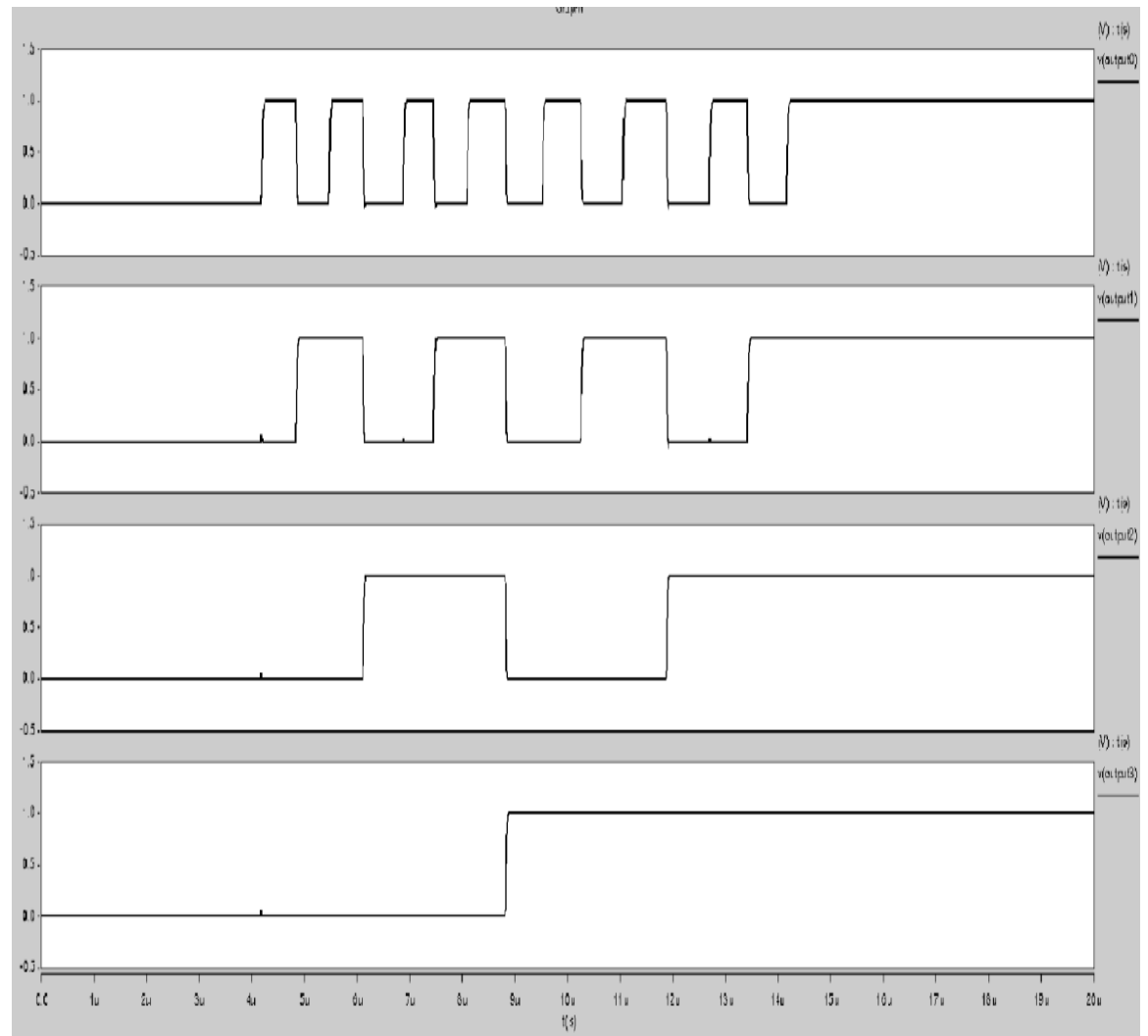
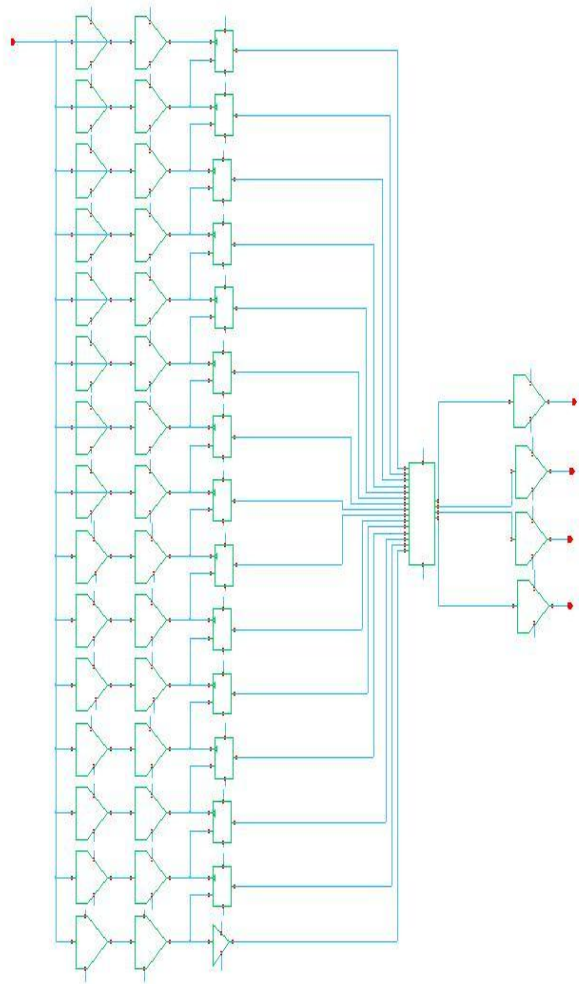
- The ADC input range varies due to process parameter changes from one fabrication to another fabrication
- The inverter input is single ended, not differential, causing the ADC to become more susceptible to noise



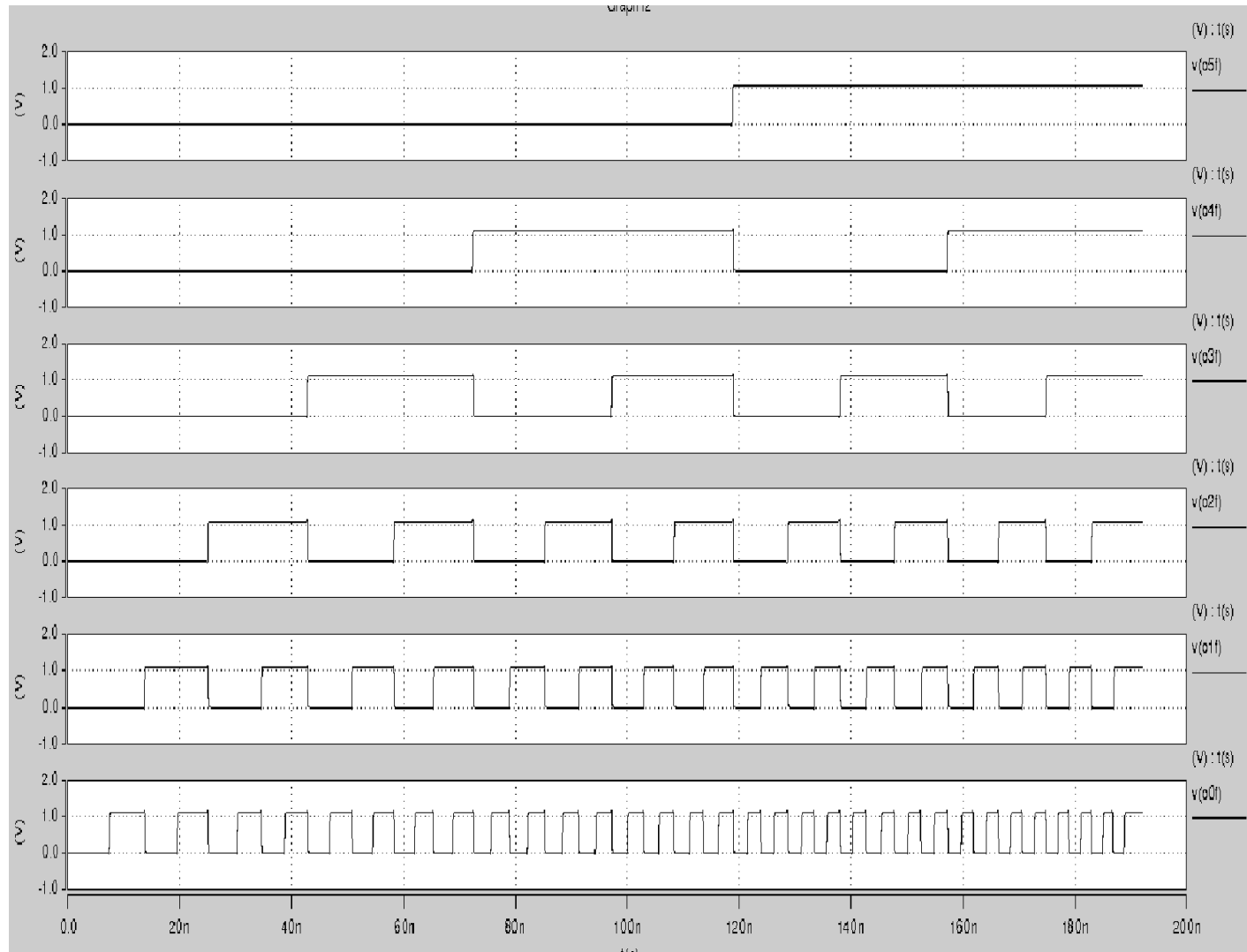
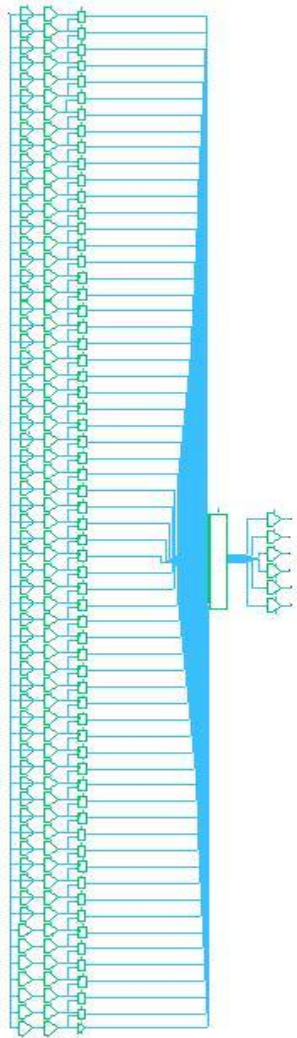
Simulation results for 3 bit TIQ ADC



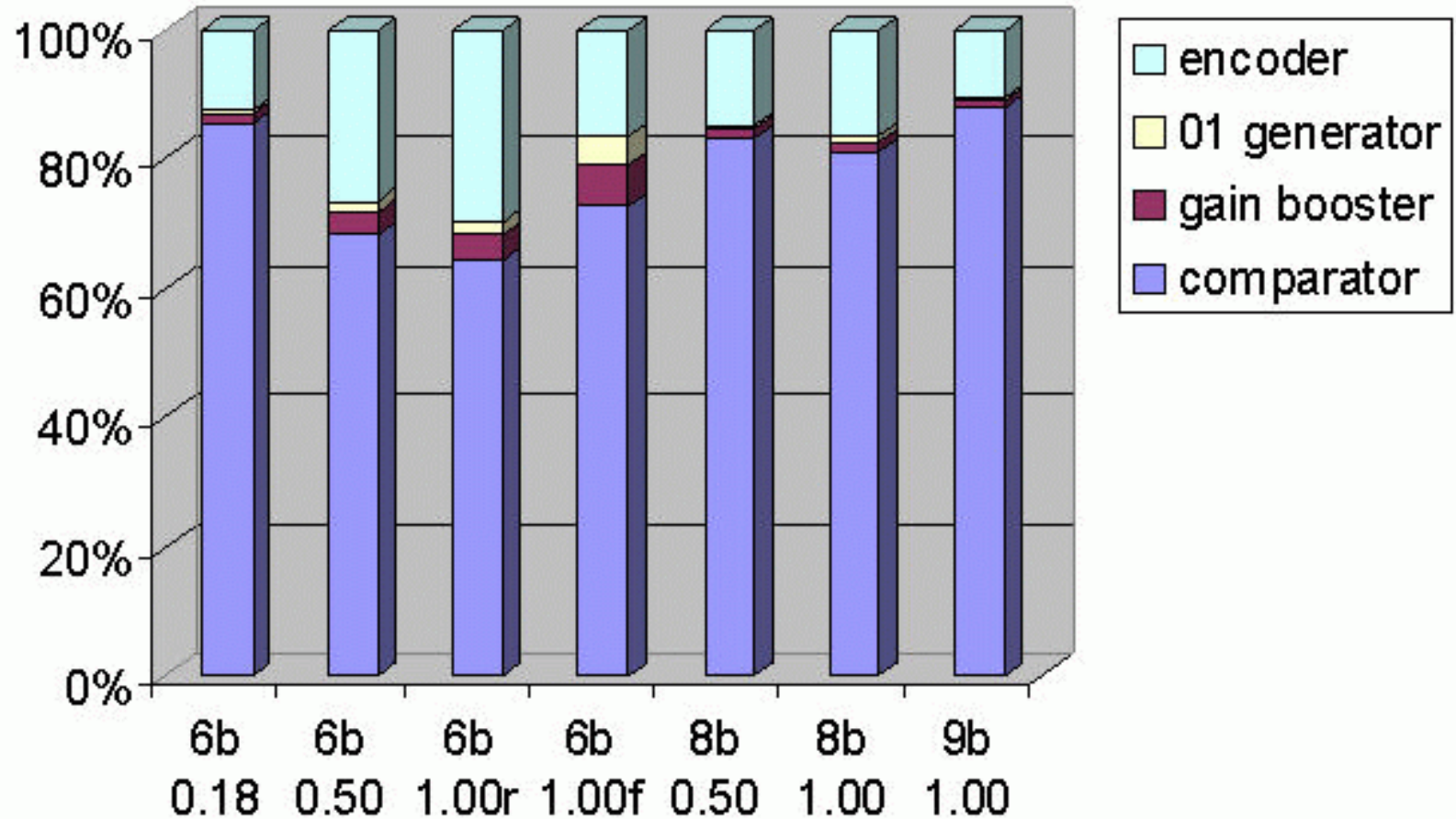
Simulation results for 4 bit TIQ ADC



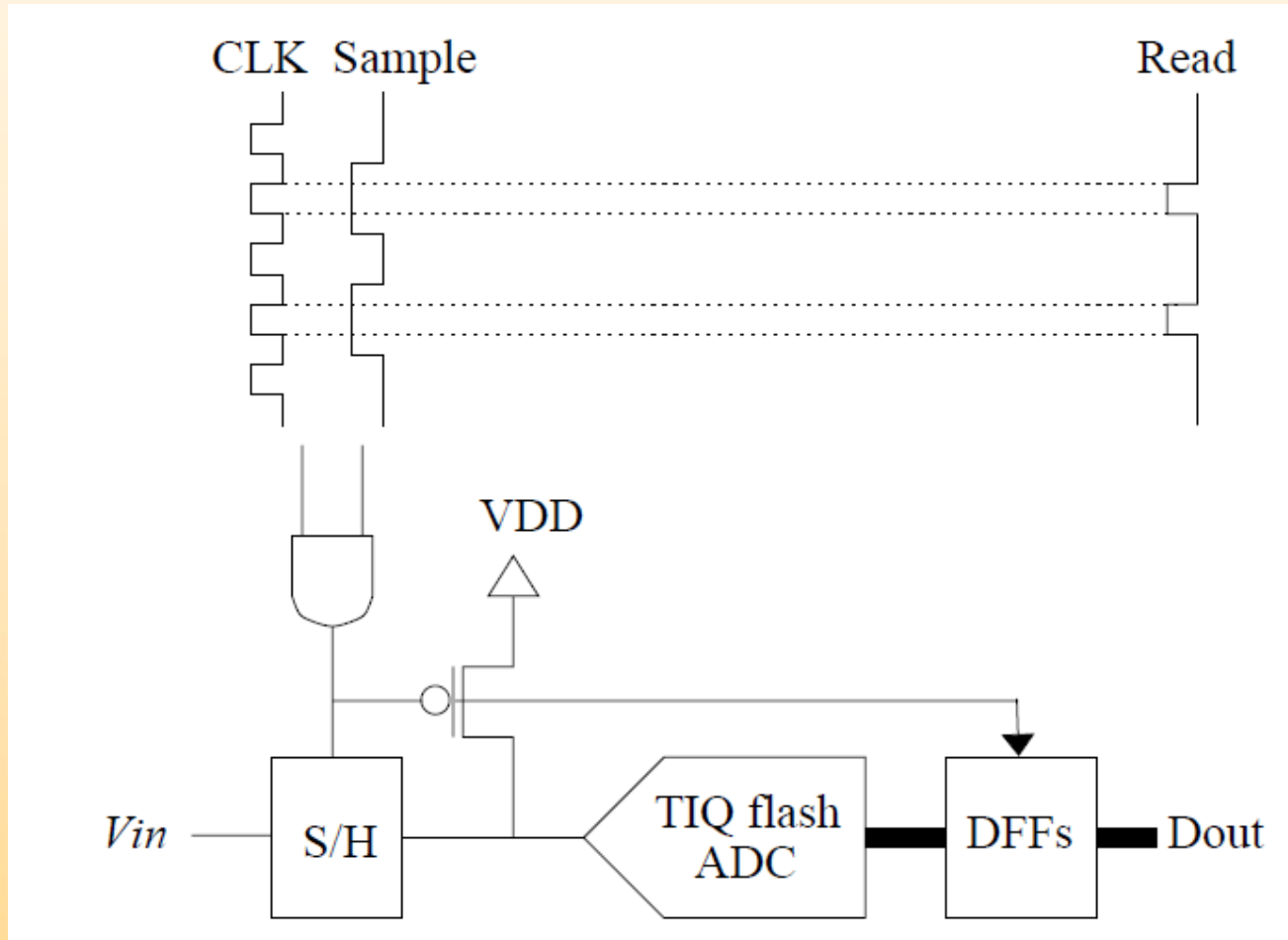
Simulation results for 6 bit TIQ ADC



Relative currents used by each component



Power Management Method (1)



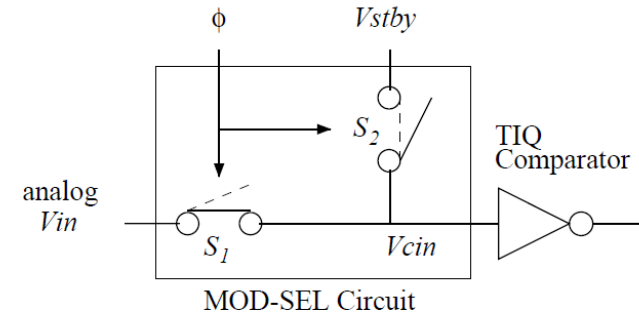
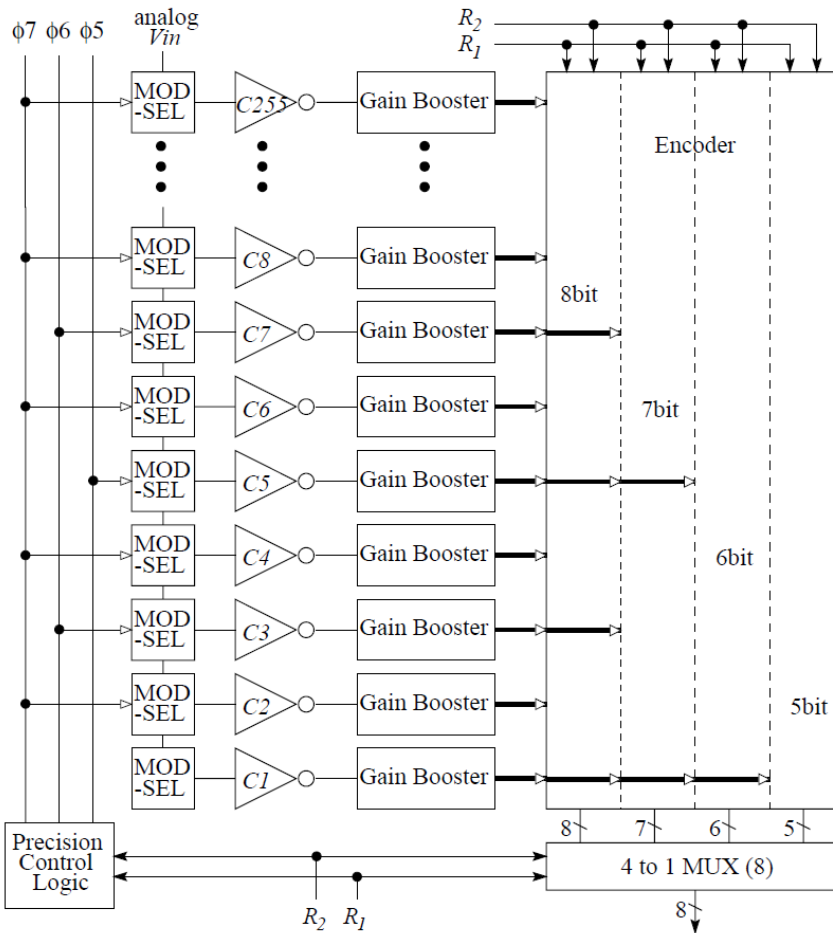
Power Management Method (2)

Sampling Rate (sps)	Power (mW)
1.7G	203.7
161.3M	69.38
32.3M	14.1
6.5M	3.37
1.3M	0.18

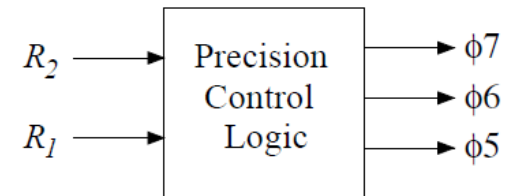
When the sampling interval was increased by 5 times, the power dissipation was proportionally reduced

Power dissipation is linearly proportional to the frequency scaling

The Power and Resolution Adaptive ADC (1)



RA-ADC Precision	$R_2 R_1$	$\phi 7$	$\phi 6$	$\phi 5$
8-bit	0 0	1	1	1
7-bit	0 1	0	1	1
6-bit	1 0	0	0	1
5-bit	1 1	0	0	0



The Power and Resolution Adaptive ADC (2)

Resolution (bits)	Power (mW)	Speed (GSPS)
6	434.63	1.25
5	223.15	1.61
4	120.29	2.22
3	68.63	3.03

- The power dissipation is reduced by almost 50% for each resolution bit reduction
- ADC speed increase as the number of resolution bits is decreased

Conclusion

- Small overhead for switching
- Unused comparators go to standby mode
- Prolong the battery-powered operation
- Linear power reduction with linear frequency scaling
- Exponential power reduction with linear resolution reduction



Thank you

