Low Power Design Methods: Design Flows and Kits

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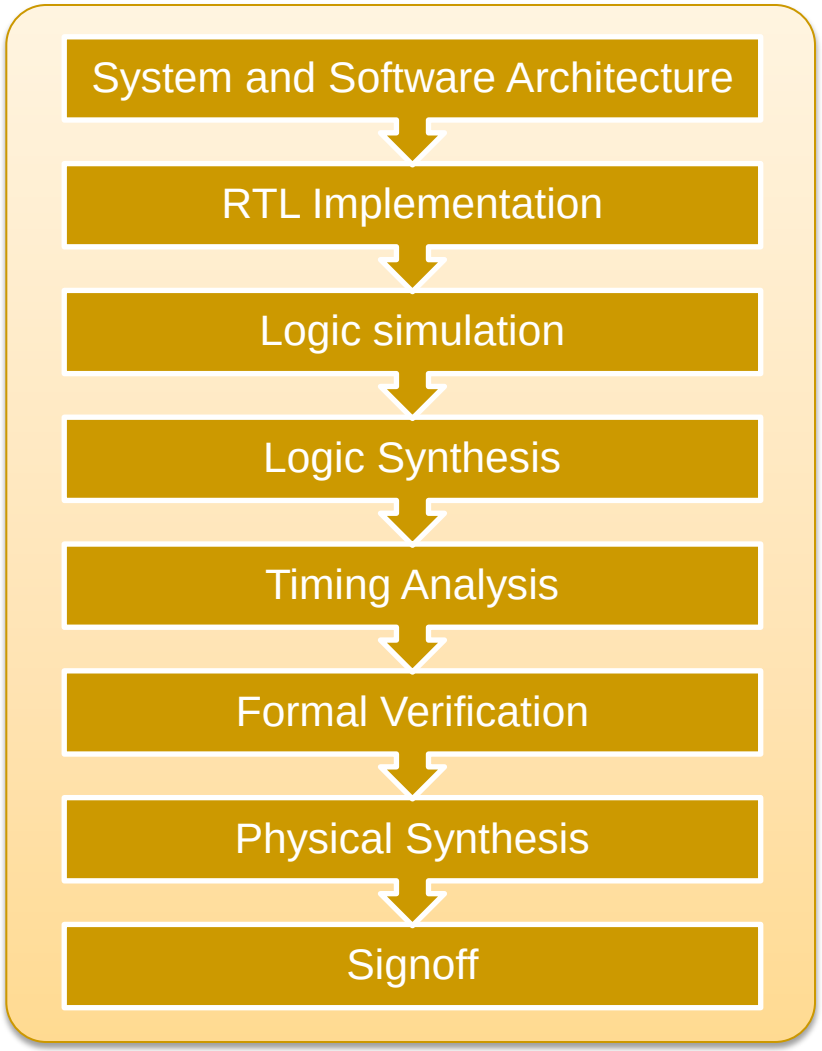
Outline

- Low Power Design Flows
- Library requirements for Low Power Design
- Example of 90nm EDK

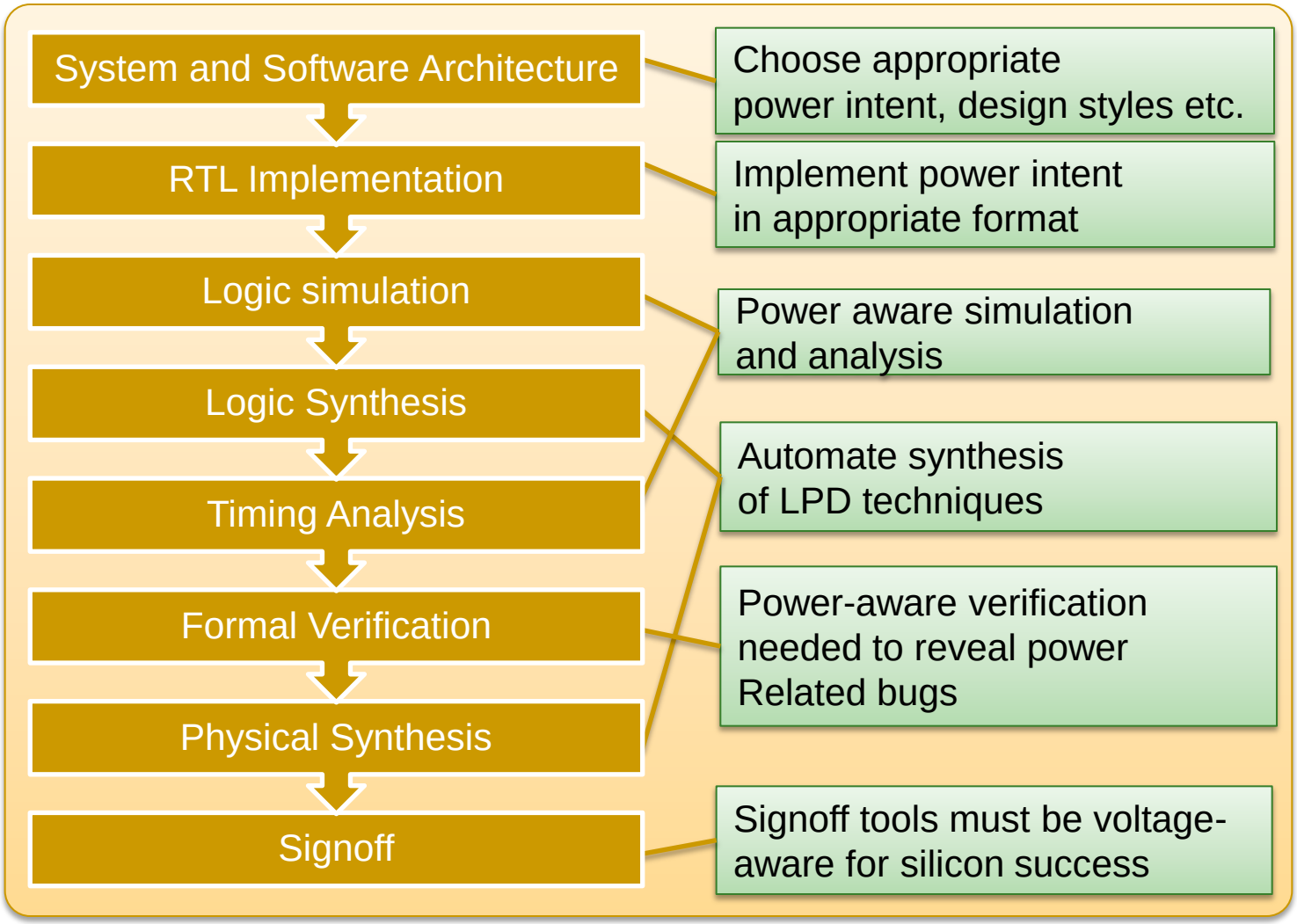
Conventional Design Flow



Power Management should be taken into account at the earliest design stages

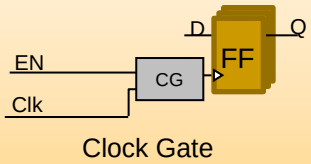
Almost every step of design flow need to be modified for LPD

Power-Aware Design Flow



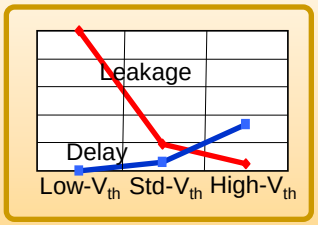
LPD Techniques Automation Levels

Clock Gating



Clock Gate

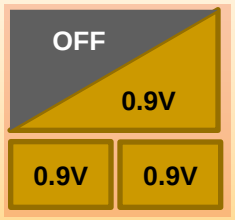
Multi-threshold



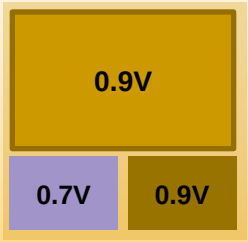
Automatically

No special treatment needed

Power gating



Multi Voltage



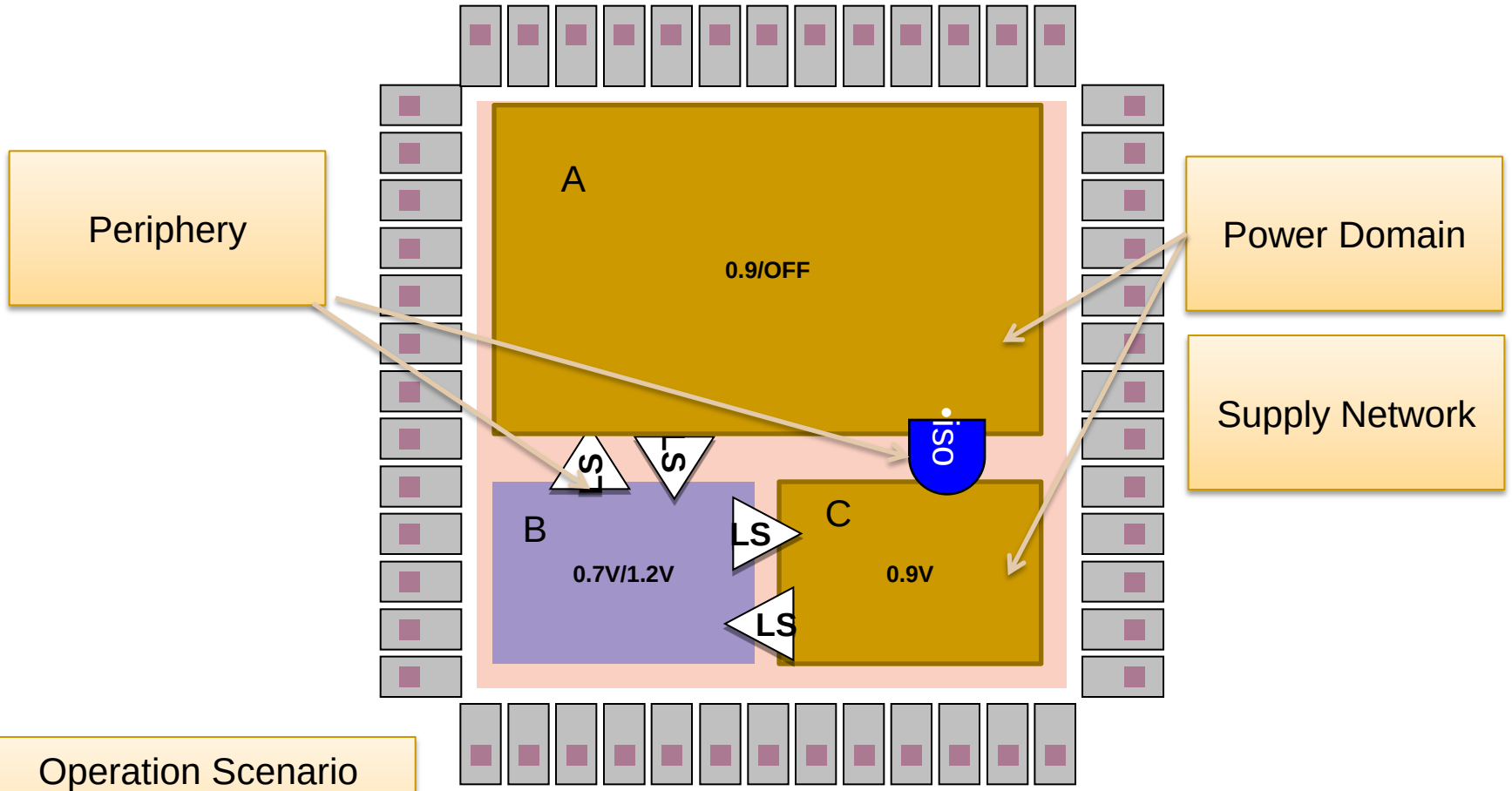
Automatically

Specification of power intent (UPF)

Unified Power Format (UPF): Necessity

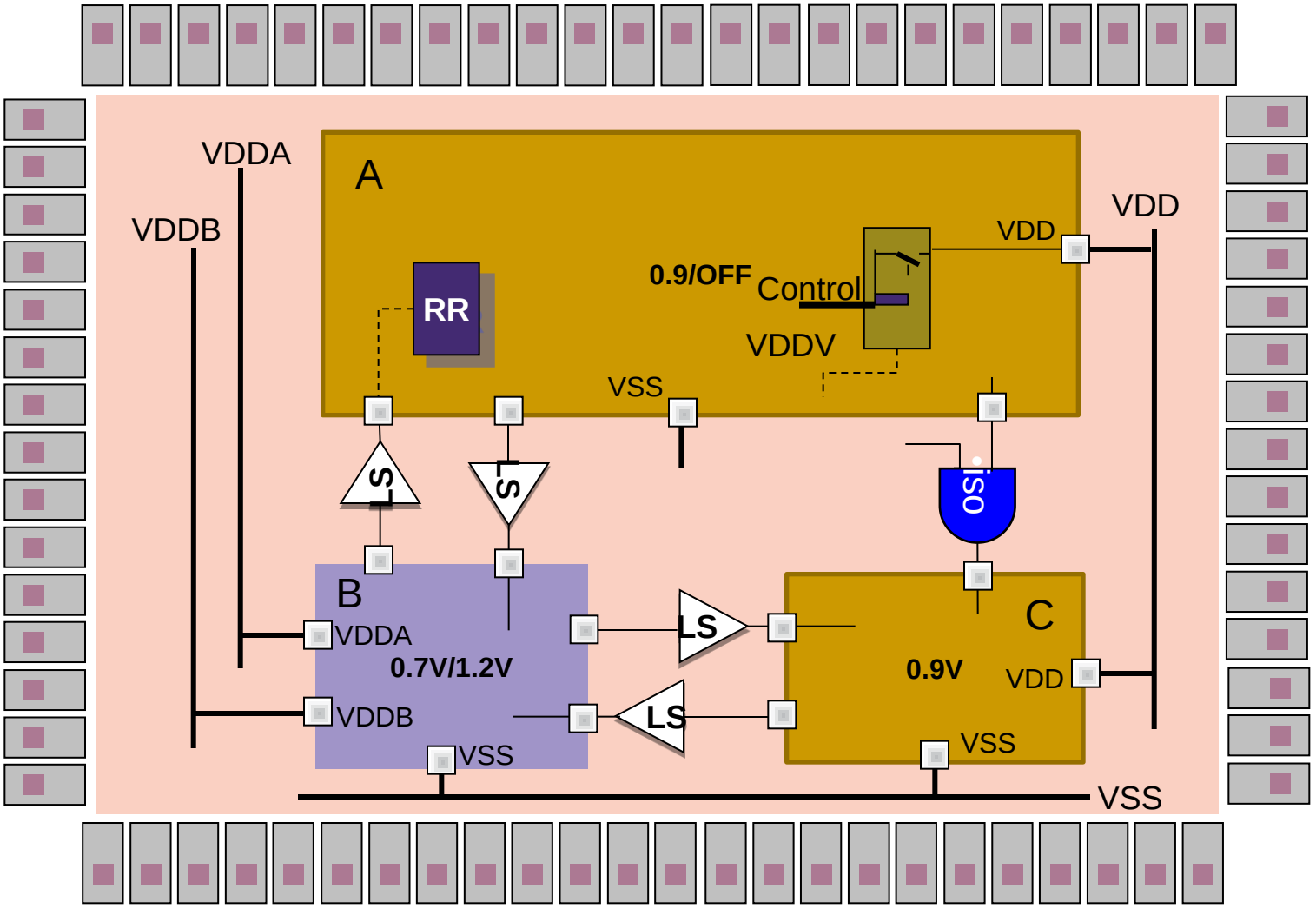
Language	Specification of power intent	Interoperable among EDA tools	Can be freely used (open standard)
Hardware Description Languages (Verilog, VHDL, etc.)	-	+	+
Vendor –Specific Formats	+	-	-
UPF	+	+	+

Specifying Power Intent

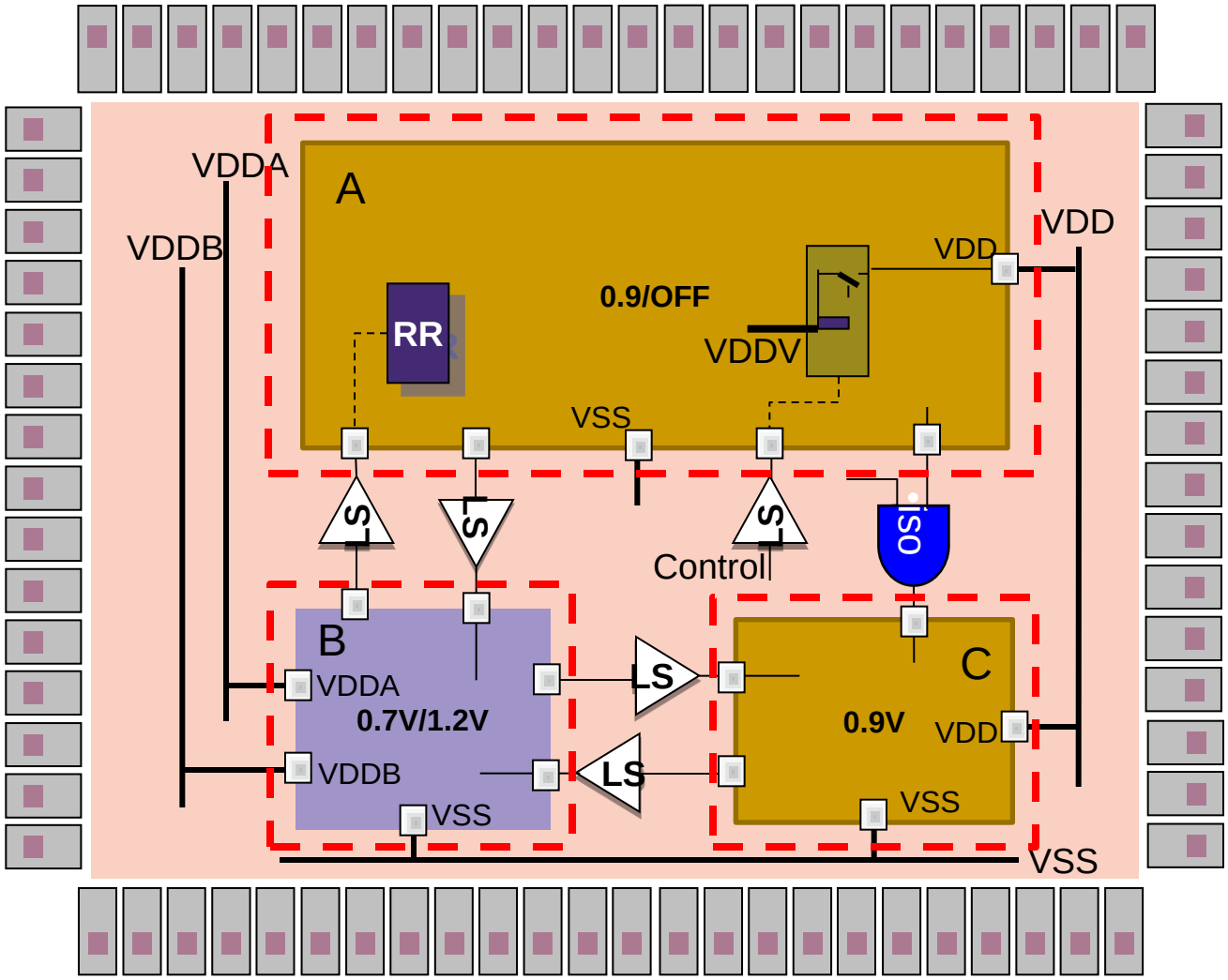


MV with power gating

MV with Power Gating Example

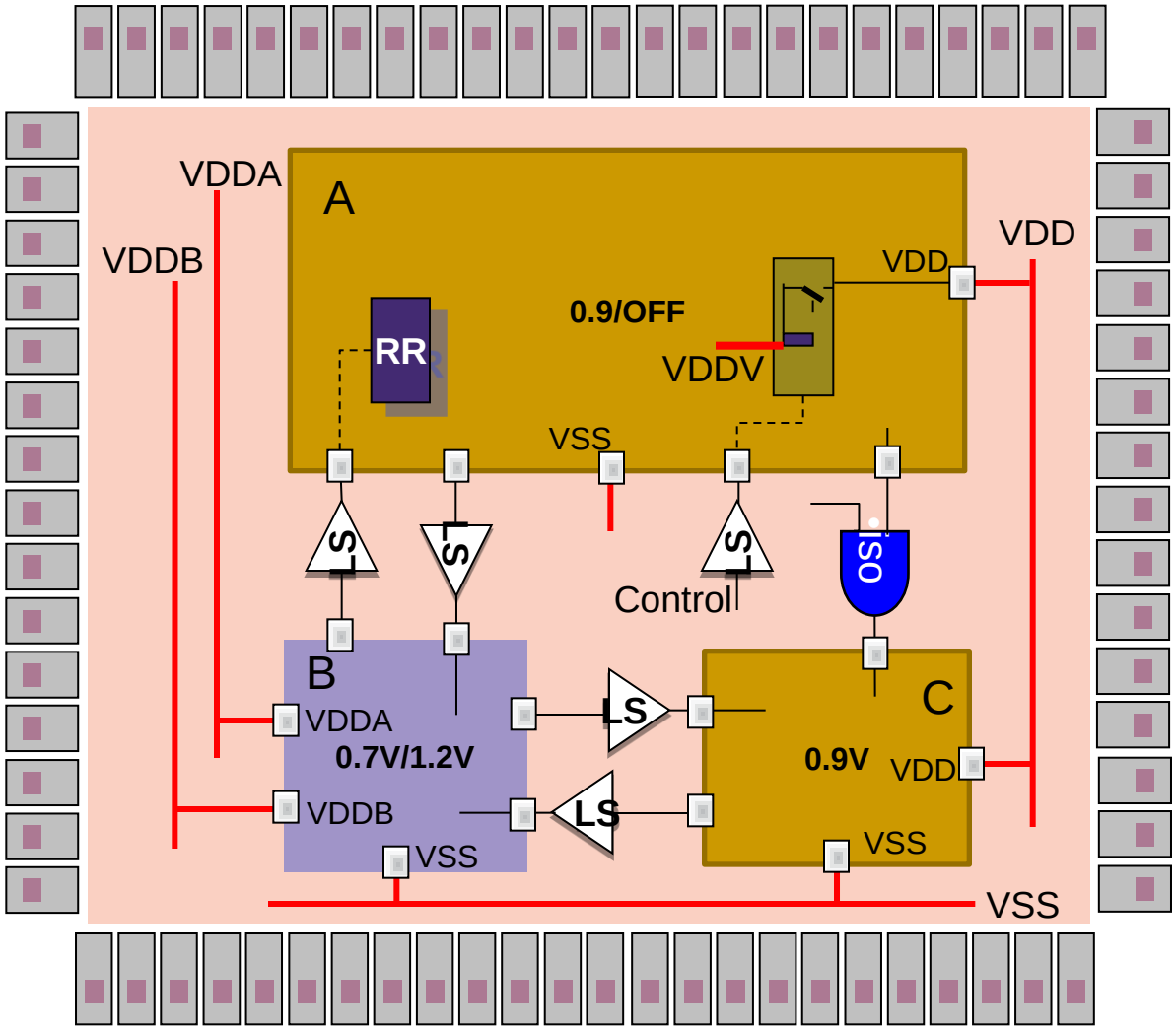


UPF: Power Domains



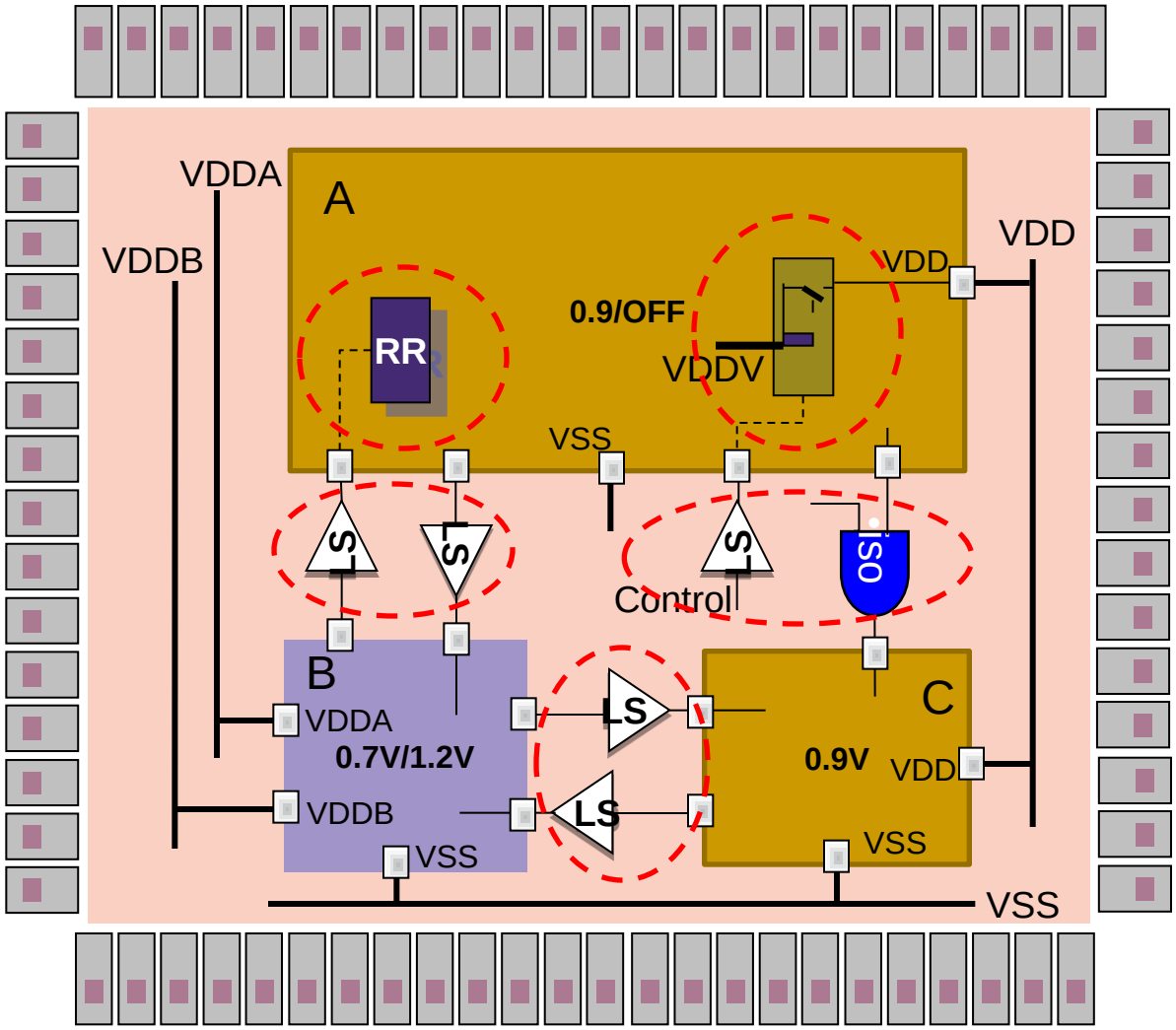
UPF	
Power Domain	**Power State**
A	0.9/OFF
B	0.7/1.2
C	0.9

UPF: Supply Network



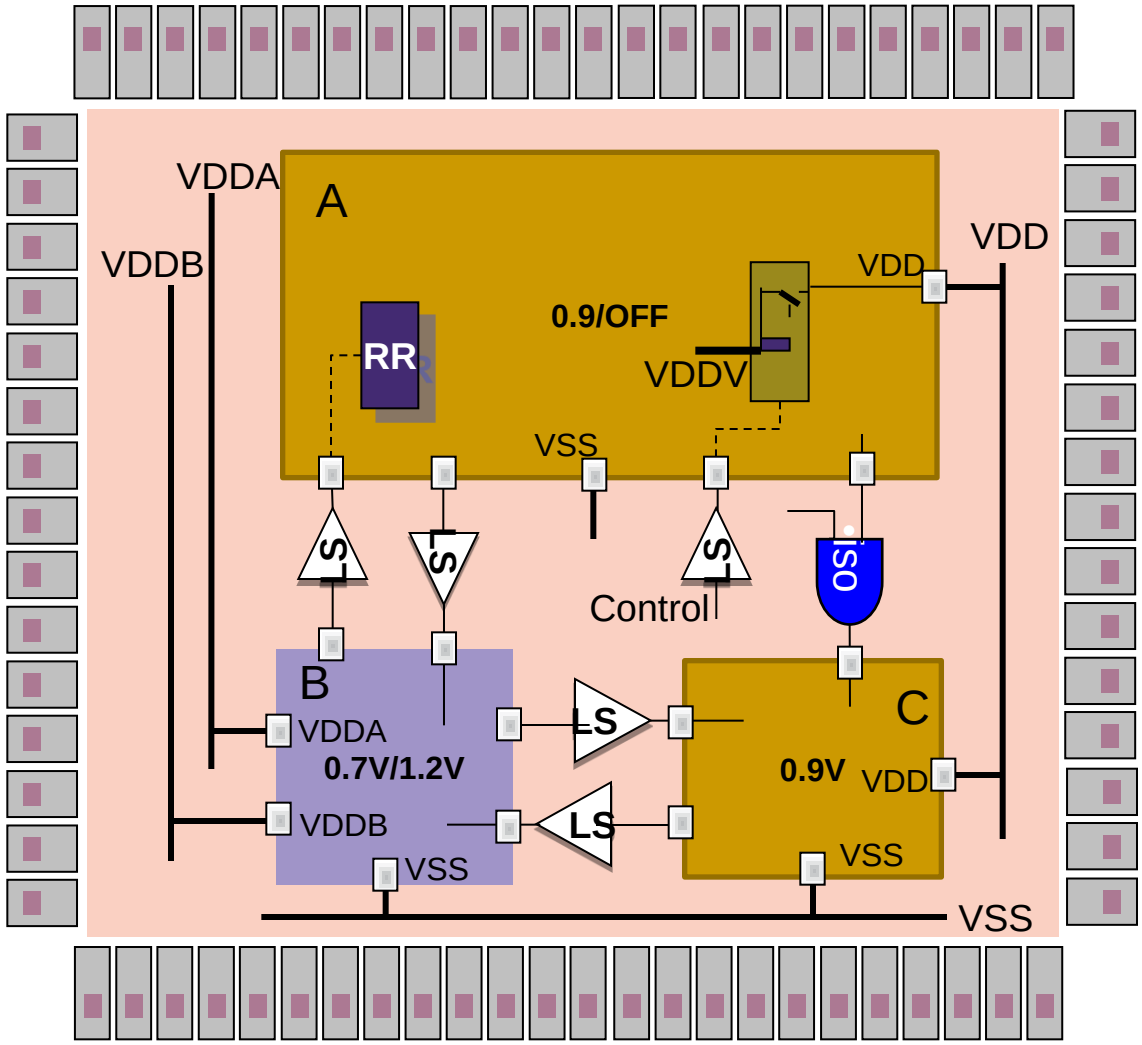
UPF		
Supply Net	**Voltage Level (V)**	**Power Domain**
VDD	0.9	C
VDDA	0.7	B
VDDB	1.2	B
VDDV	Virtual 0.9	A
VSS	Common Ground	A/B/C

UPF: Periphery



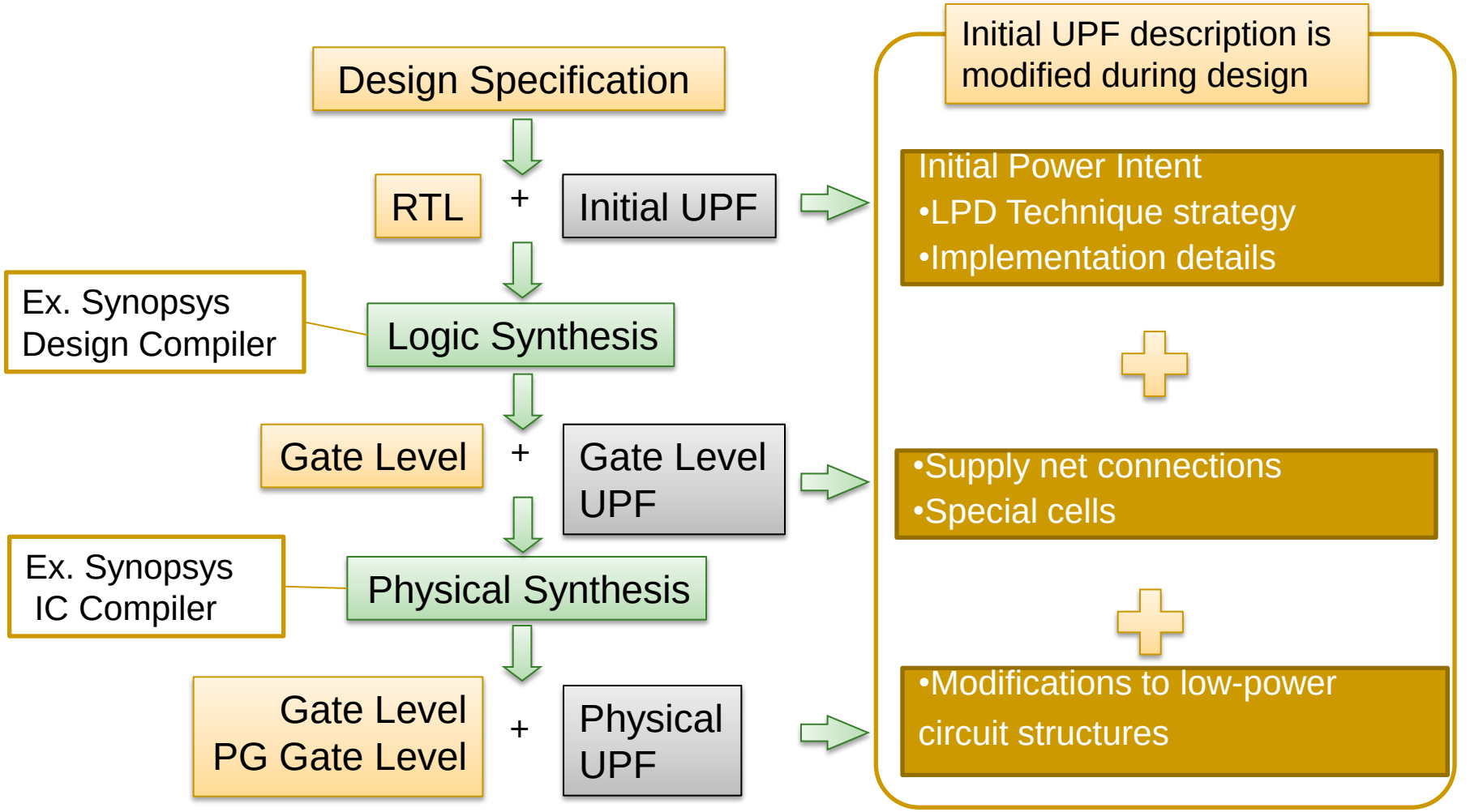
UPF
Required Periphery
Level Shifters between A and B
Level Shifters between B and C
Isolation between C and A
Retention Cell inside A
Control Block inside A

UPF: State Scenario



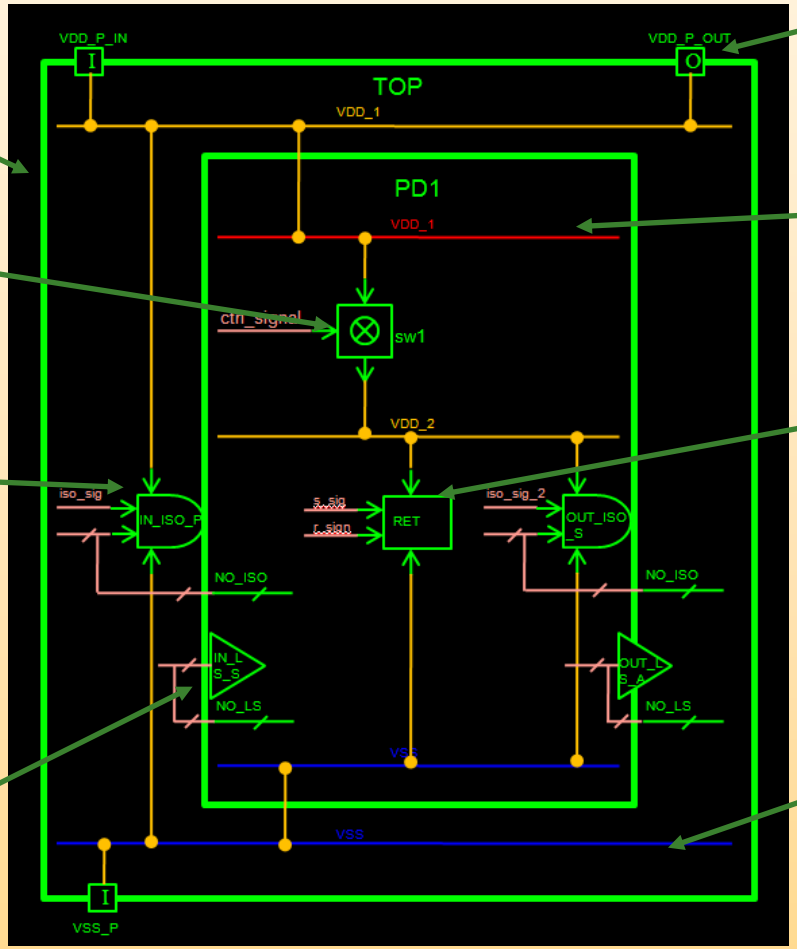
UPF			
A	B	C	Scenario
0.9	0.7	0.9	Allowed
0.9	1.2	0.9	Allowed
OFF	0.7	0.9	Allowed
OFF	1.2	0.9	Not Allowed

Design Flow Modification with UPF



Design Compiler Visual UPF

Strategies Visualization



PD boundary

Power Switch

ISO location parentwith backup power defined

LS strategy defined in UPF

Supply port

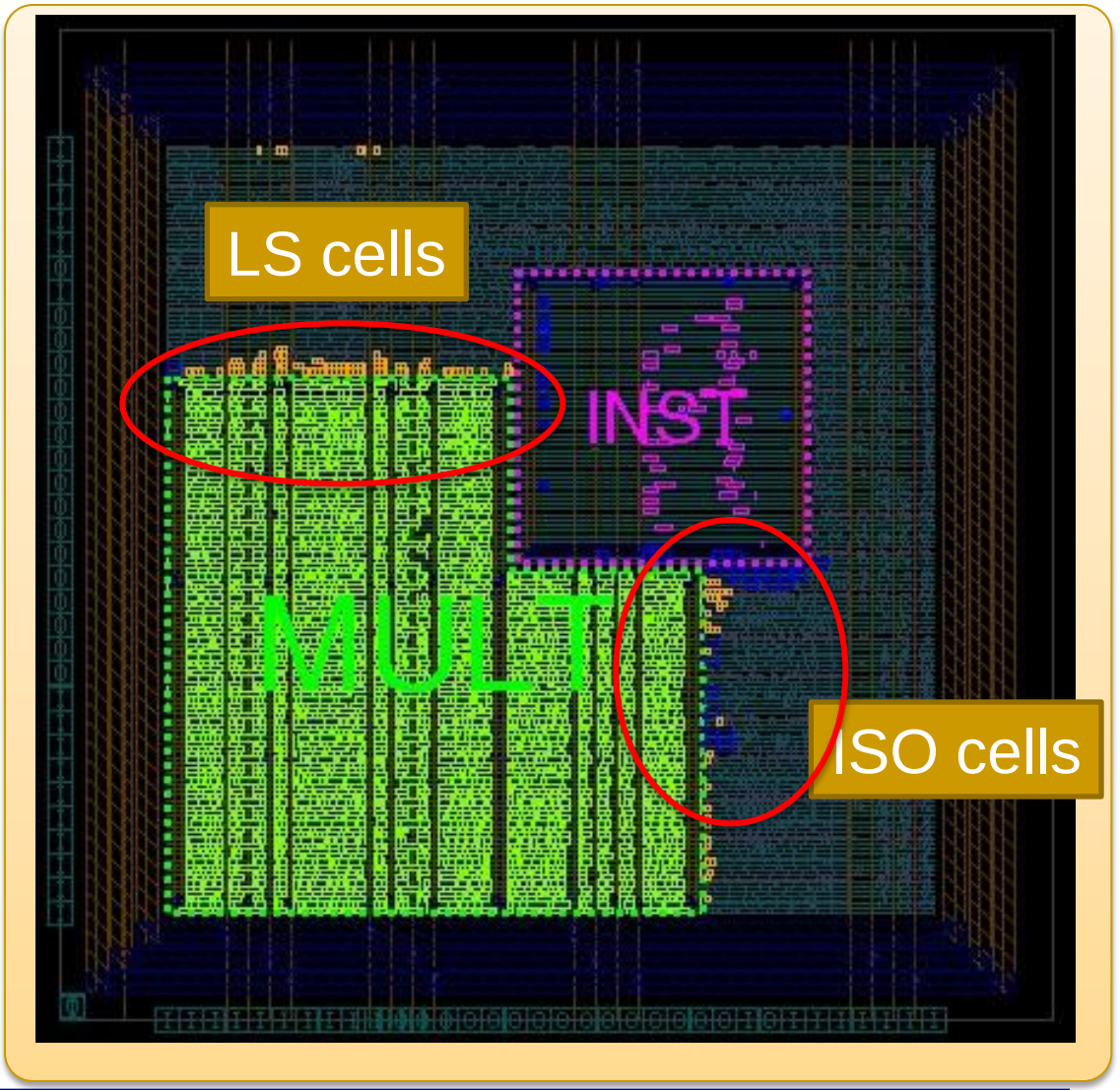
Block PD primary power net

Retention register

Top PD primary ground net

IC Compiler UPF Placement

- Placement respects voltage area boundary
- Special Level Shifter and Isolation Cells placement
  - Special cells placed closer to VA boundary



Library Requirements for LPD

- Special cells
- Special versions of library
- Characterization in additional corners
- Additional views/files/attributes

90nm EDK: Digital Standard Cell Library

Digital Standard Cell Library (DSCL)

Aimed at optimizing the main characteristics of designed Ics

Contains 340 cells, cell list compiled based on the requirements for educational designs

Typical combinational and sequential logic cells for different drive strengths

Typical combinational and sequential

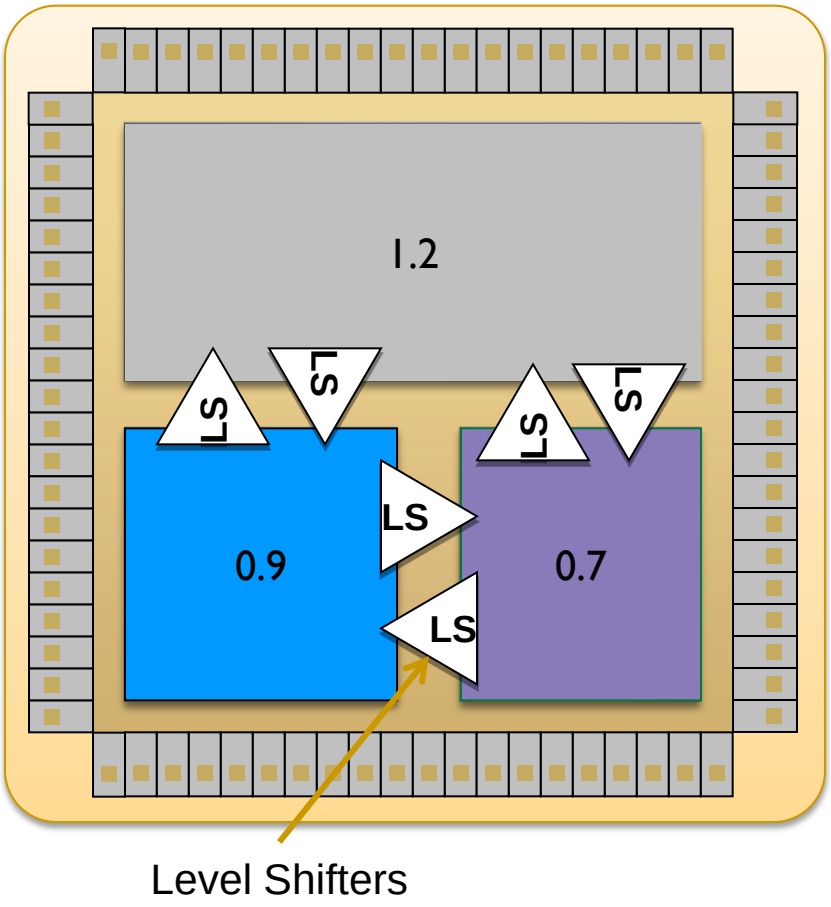
Inverters/Buffers	Logic Gates	Flip-Flops (regular+scan)
Latches	Delay Lines	Physical (Antenna diode)

Special cells for different styles LPD

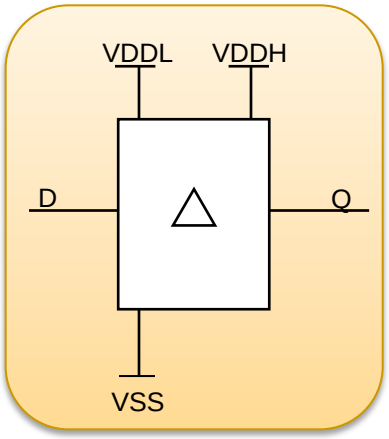
Isolation Cells	Level Shifters	Retention Flip-Flops
Clock gating	Always-on Buffers	Power Gating

Provides the support of IC design with different core voltages to minimize dynamic and leakage power.

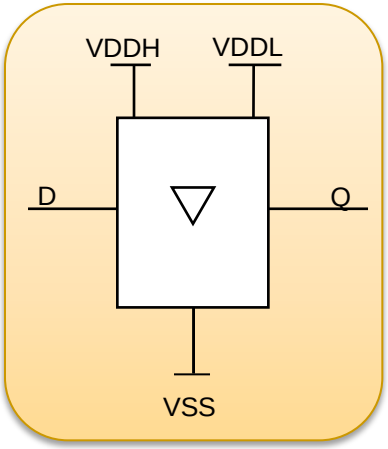
Special Cells for LPD: Level Shifter



Level Shifter



Logic Symbol of Low to High Level Shifter



Logic Symbol of High to Low Level Shifter

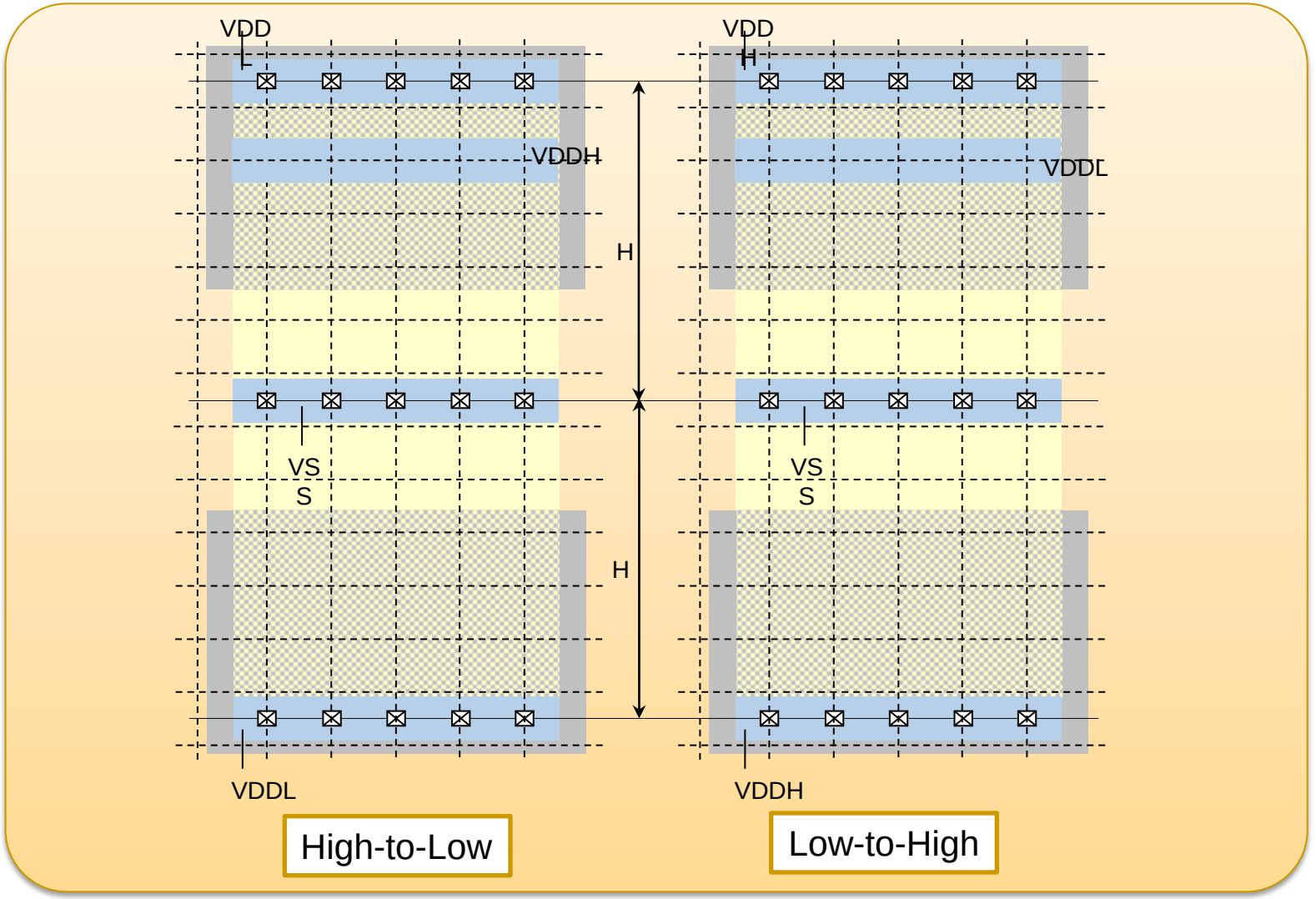
Low to High Level Shifter Truth Table

D (0.8V)	Q (1.2V)
0	0
1	1

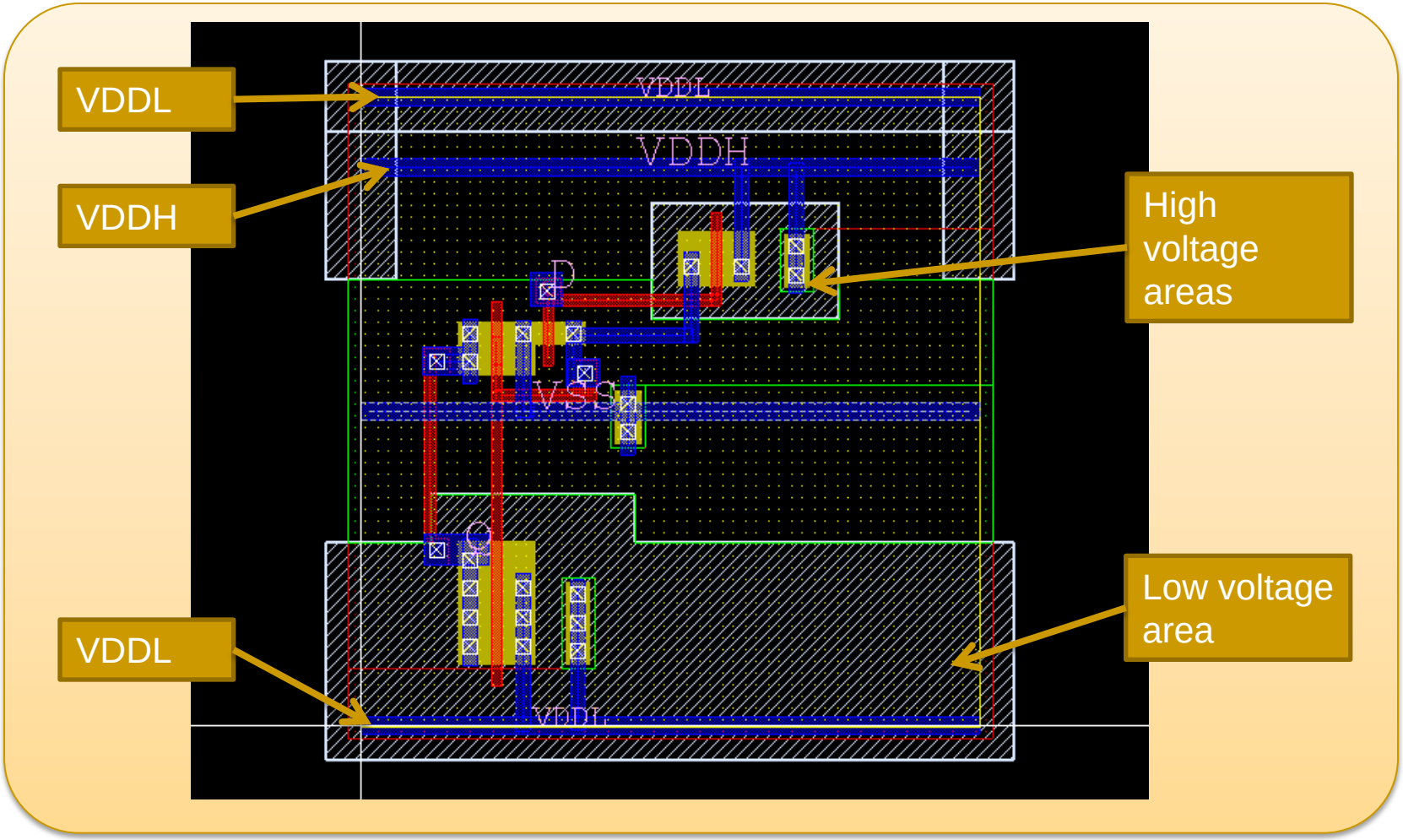
High to Low Level Shifter Truth Table

D (1.2V)	Q (0.8V)
0	0
1	1

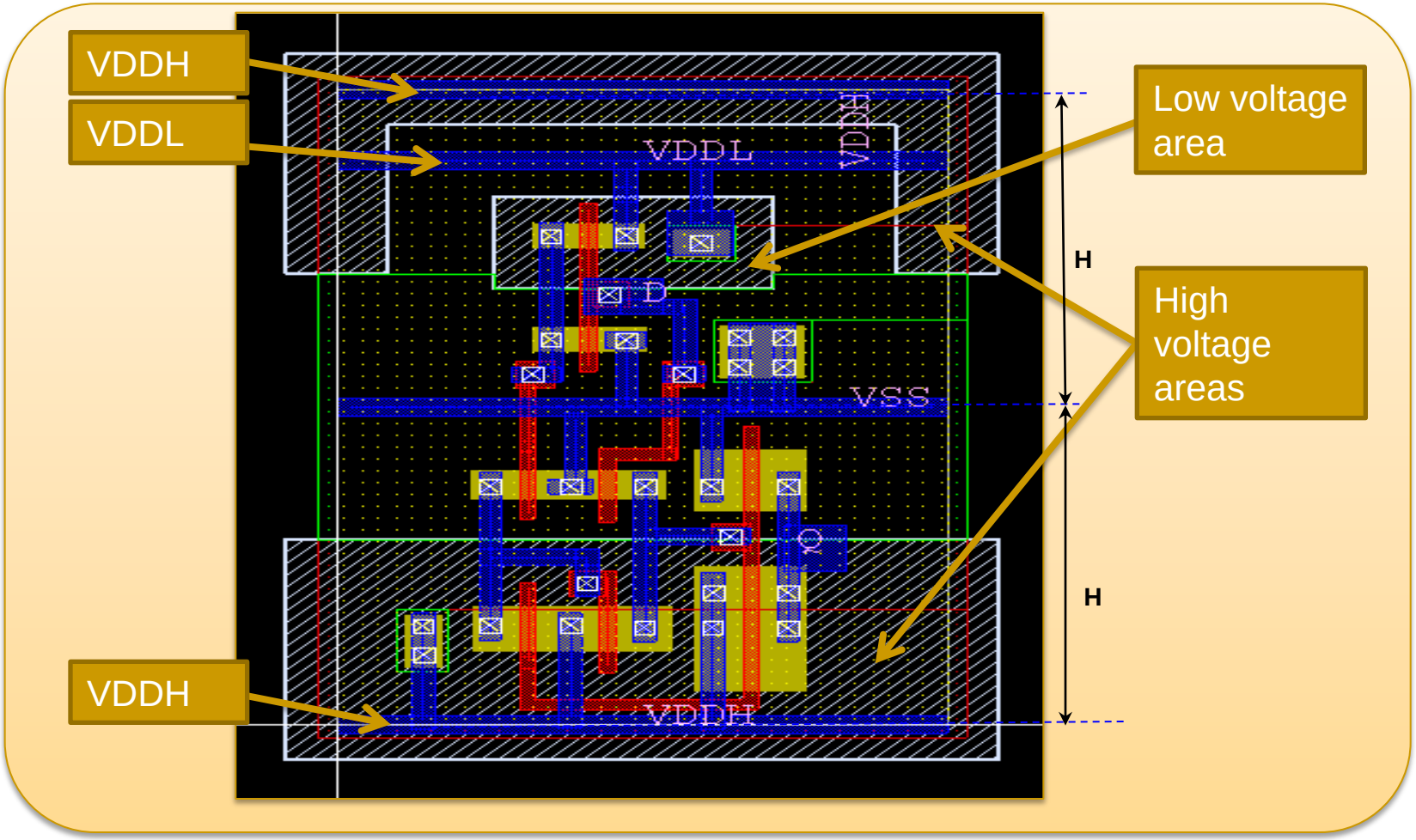
Level Shifter Physical Structure



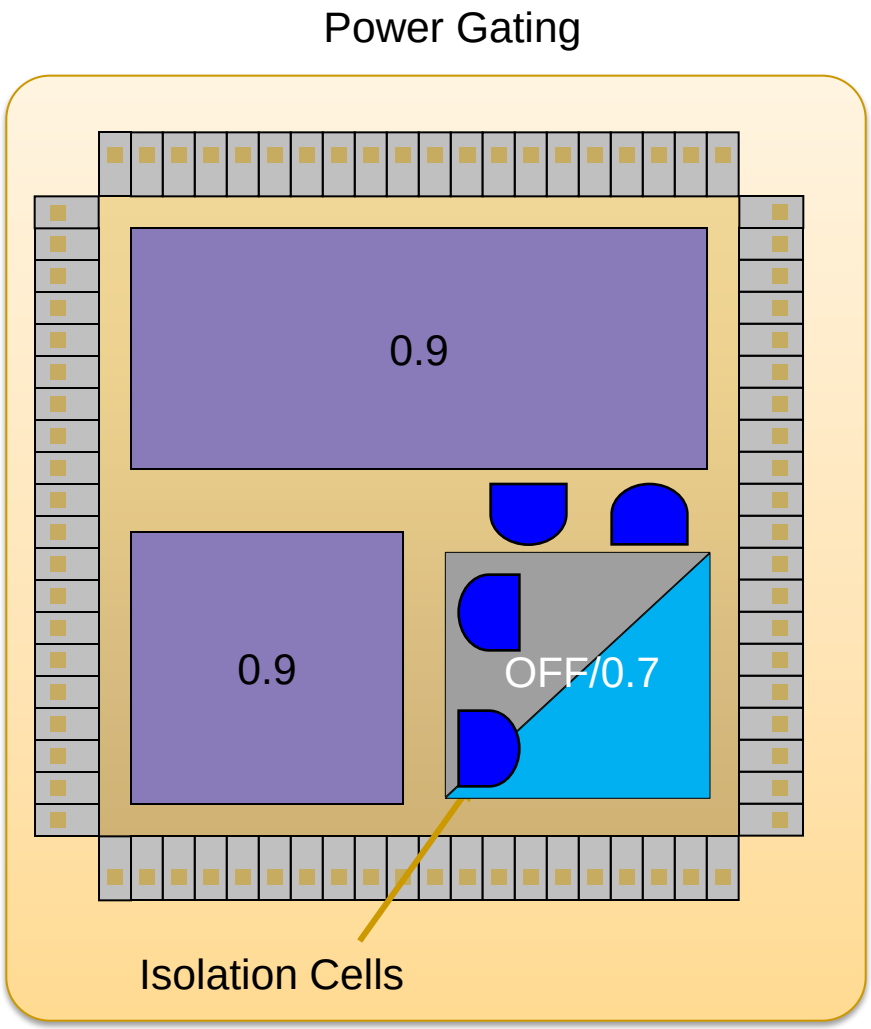
Level Shifter (High to Low) Physical Design



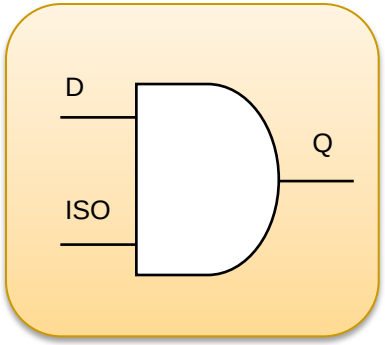
Level Shifter (Low to High) Physical Design



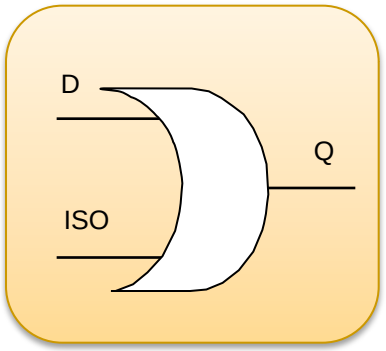
Special Cells for LPD: Isolation Cells



Isolation Cells



Logic Symbol of Clamp 0
Isolation Cell (Logic AND)



Logic Symbol of Clamp 1
Isolation Cell (Logic OR)

Hold 0 Isolation Cell (Logic AND) Truth Table

D	ISO	Q
0	1	0
1	1	1
X	0	0

Bypass mode

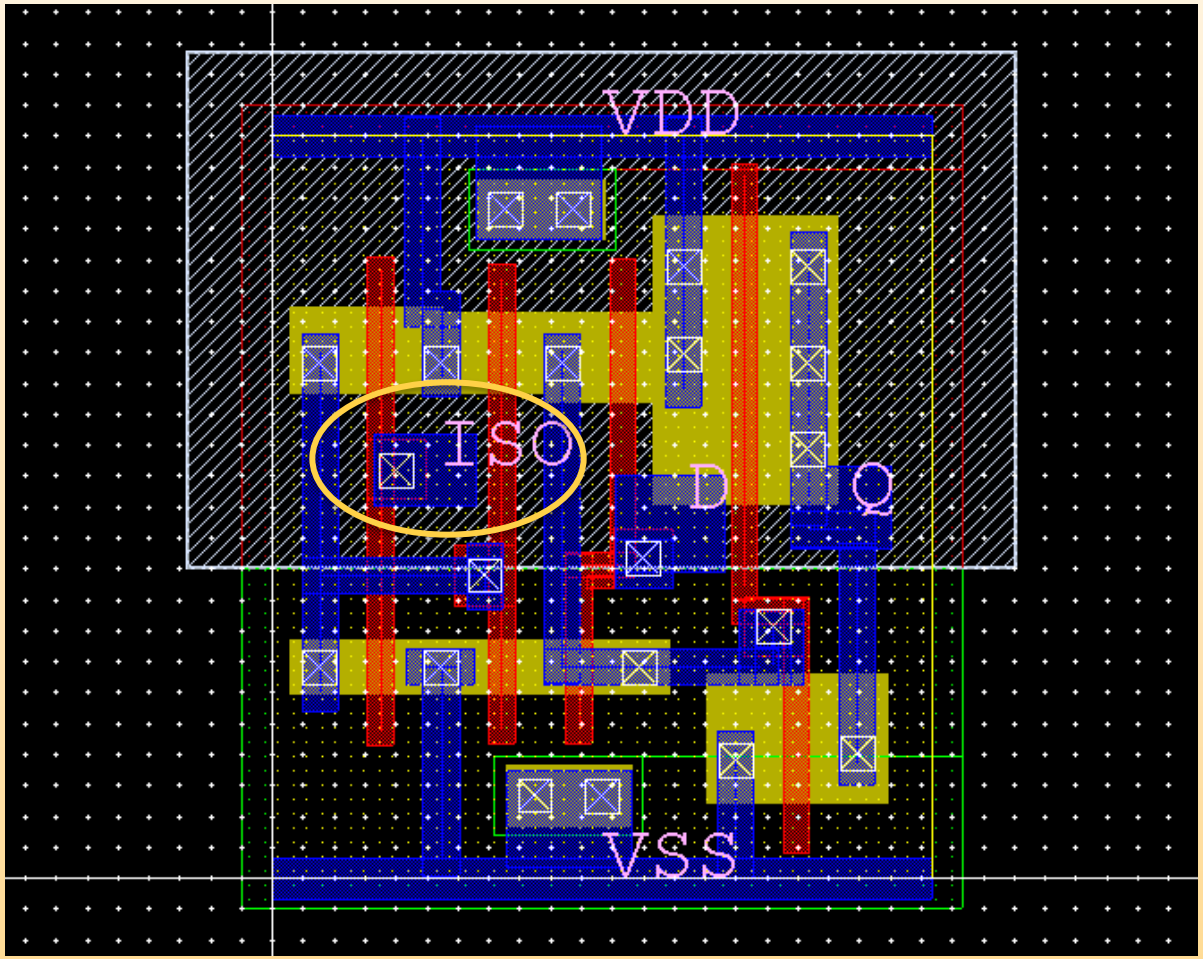
Hold 1 Isolation Cell (Logic OR) Truth Table

D	ISO	Q
0	0	0
1	0	1
X	1	1

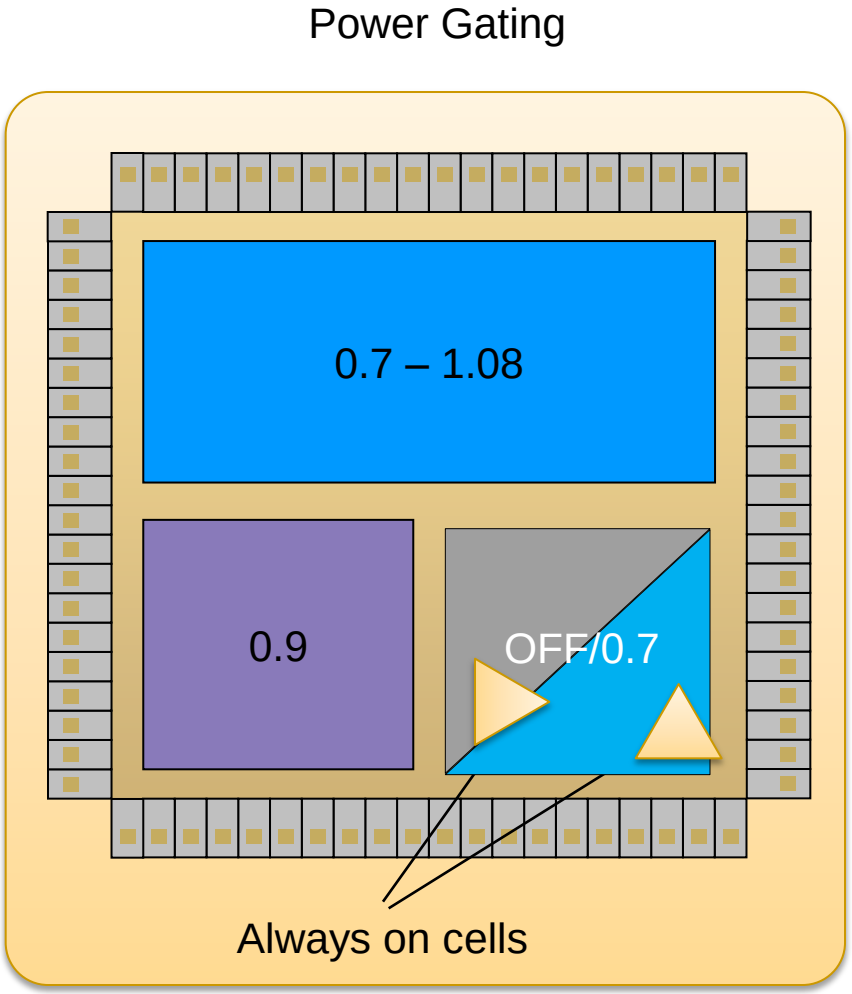
Bypass mode

Output clamped

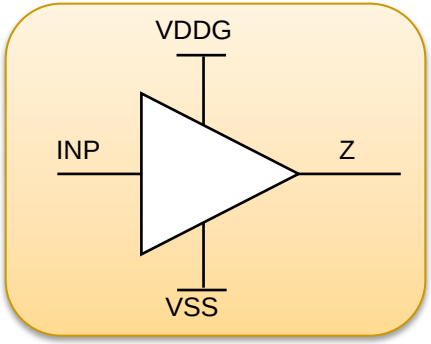
Isolation Cells: Physical Design



Special Cells for LPD: Always-on Buffers



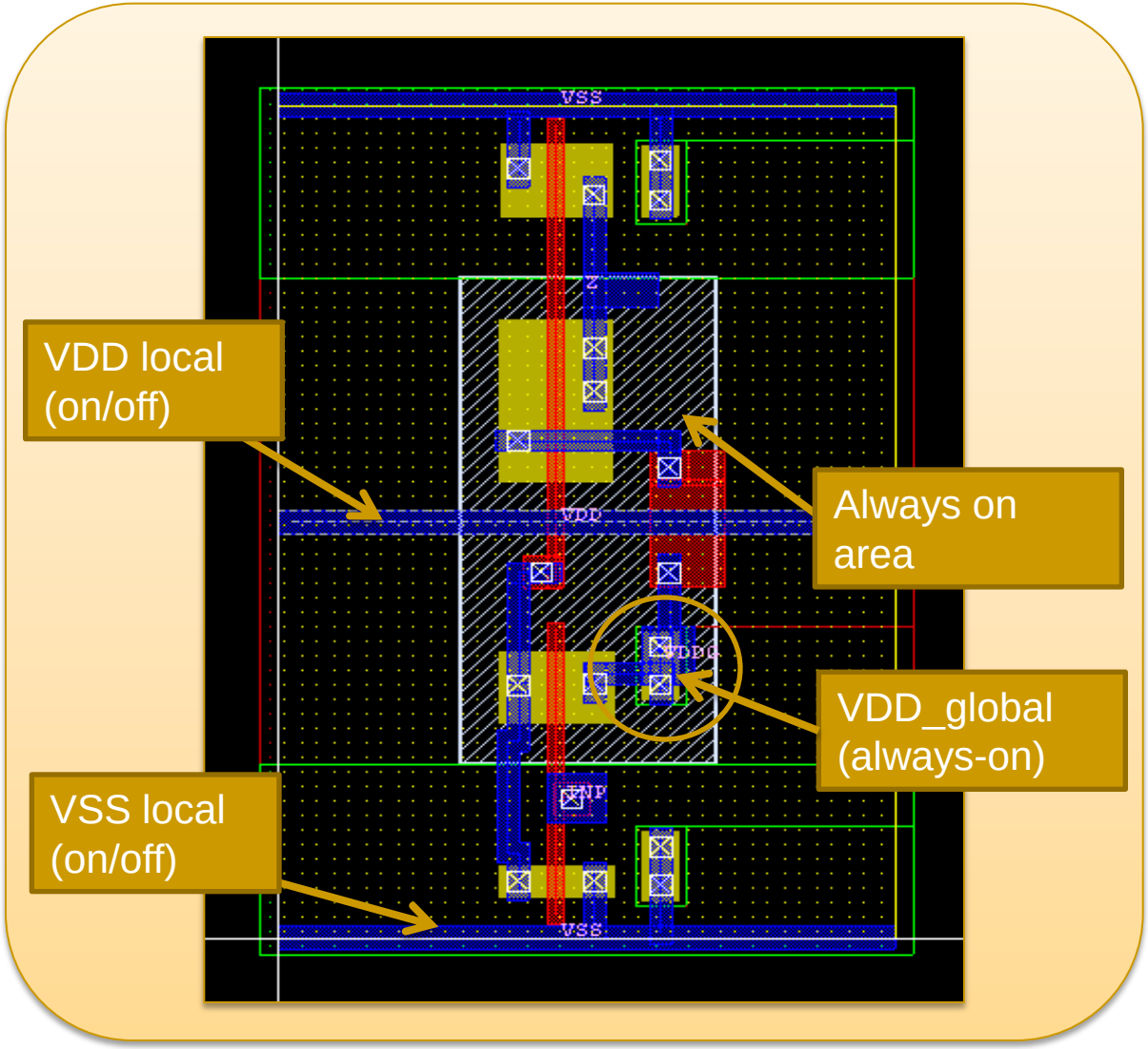
Always-on Buffer



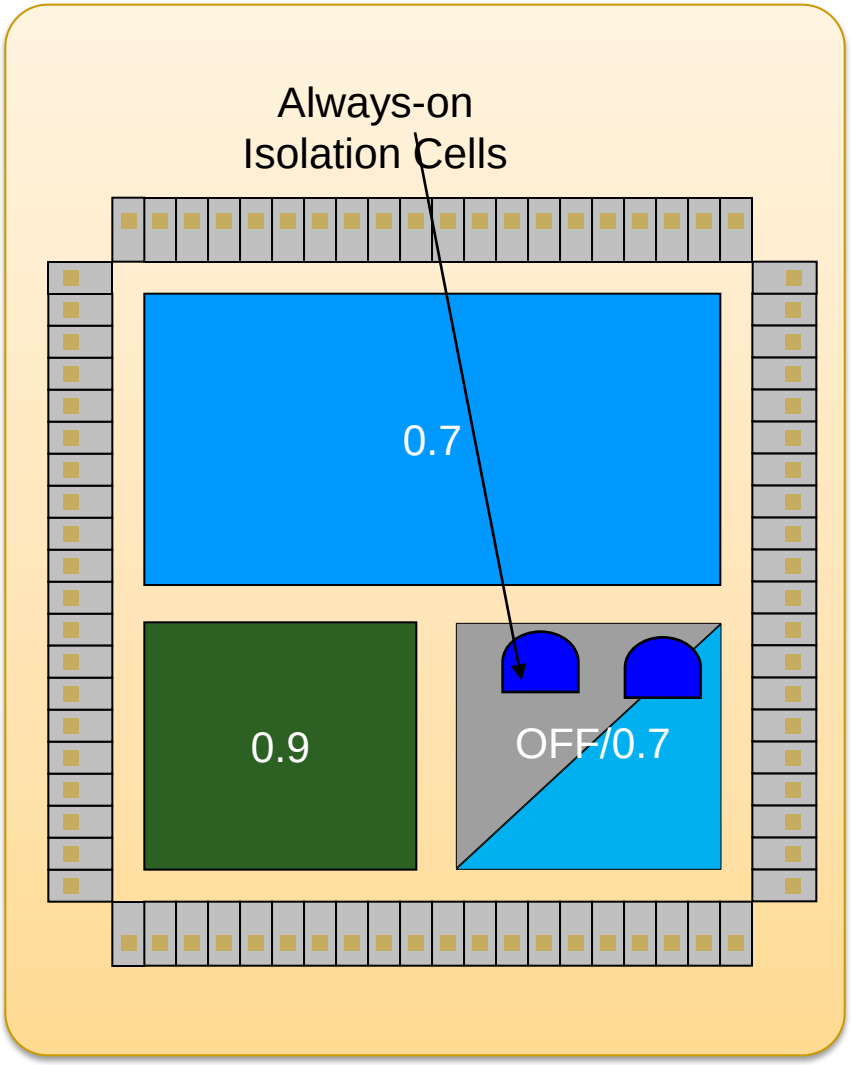
Logic Symbol of Always on Non-Inverting Buffer

Always on Non-Inverting Buffer Truth Table

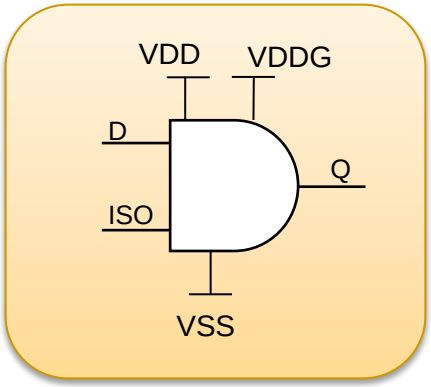
IN	VDDG	VSS	Q
0	1	0	0
1	1	0	1



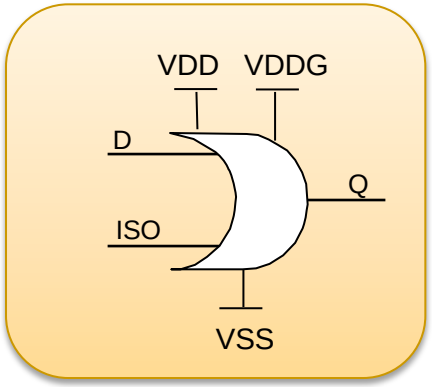
Special Cells for LPD: Always-on Isolation cells



Always on Isolation Cells



Logic Symbol of Clamp 0 Isolation Cell (Logic AND),Always On



Logic Symbol of Clamp 1 Isolation Cell (Logic OR), Always On

Hold 0 Isolation Cell (Logic AND) Truth Table

D	ISO	Q
0	1	0
1	1	1
X	0	0

Bypass mode

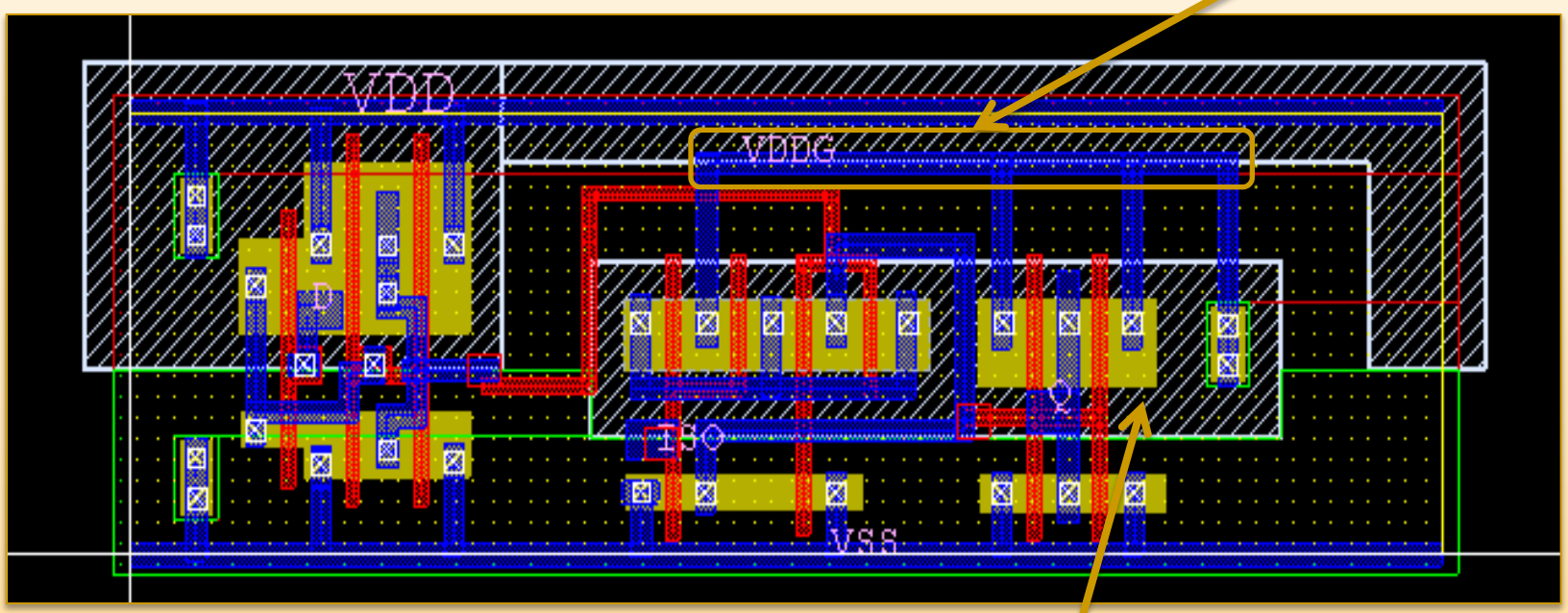
Hold 1 Isolation Cell (Logic OR) Truth Table

D	ISO	Q
0	0	0
1	0	1
X	1	1

Bypass mode

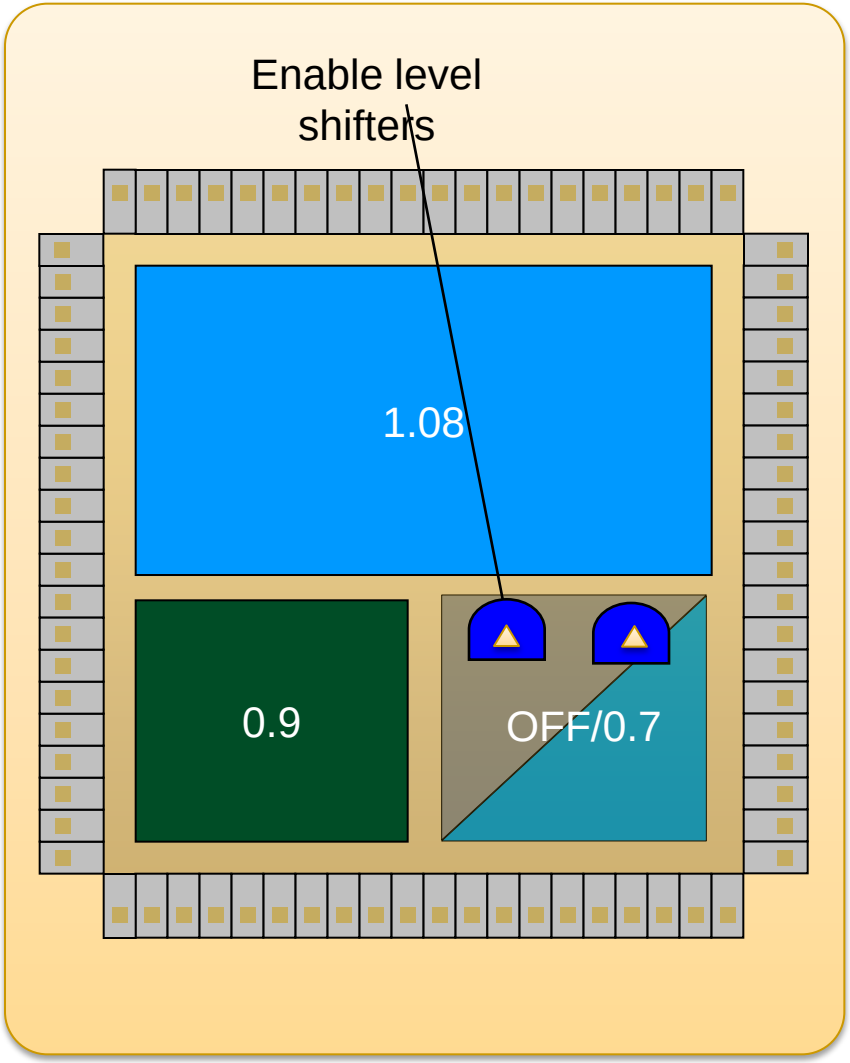
Output clamped

Isolation Cell (always-on) Physical Design

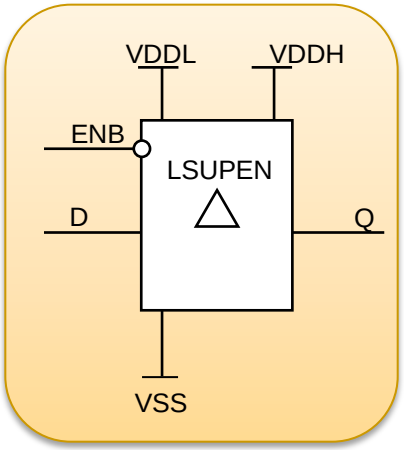


Special Cells for LPD: Enable level shifters

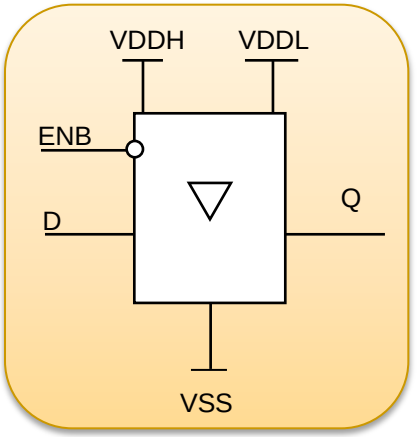
- Combination of Level Shifter and ISO cell



Level Shifters With Active Low Enable



Symbol of Low to High Level Shifter
Active Low Enable, Clamp 0



Symbol of High to Low Level Shifter
Active Low Enable, Clamp 1

D(0.8V)	ENB	Q(1.2V)
0	1	0
1	1	1
X	0	0

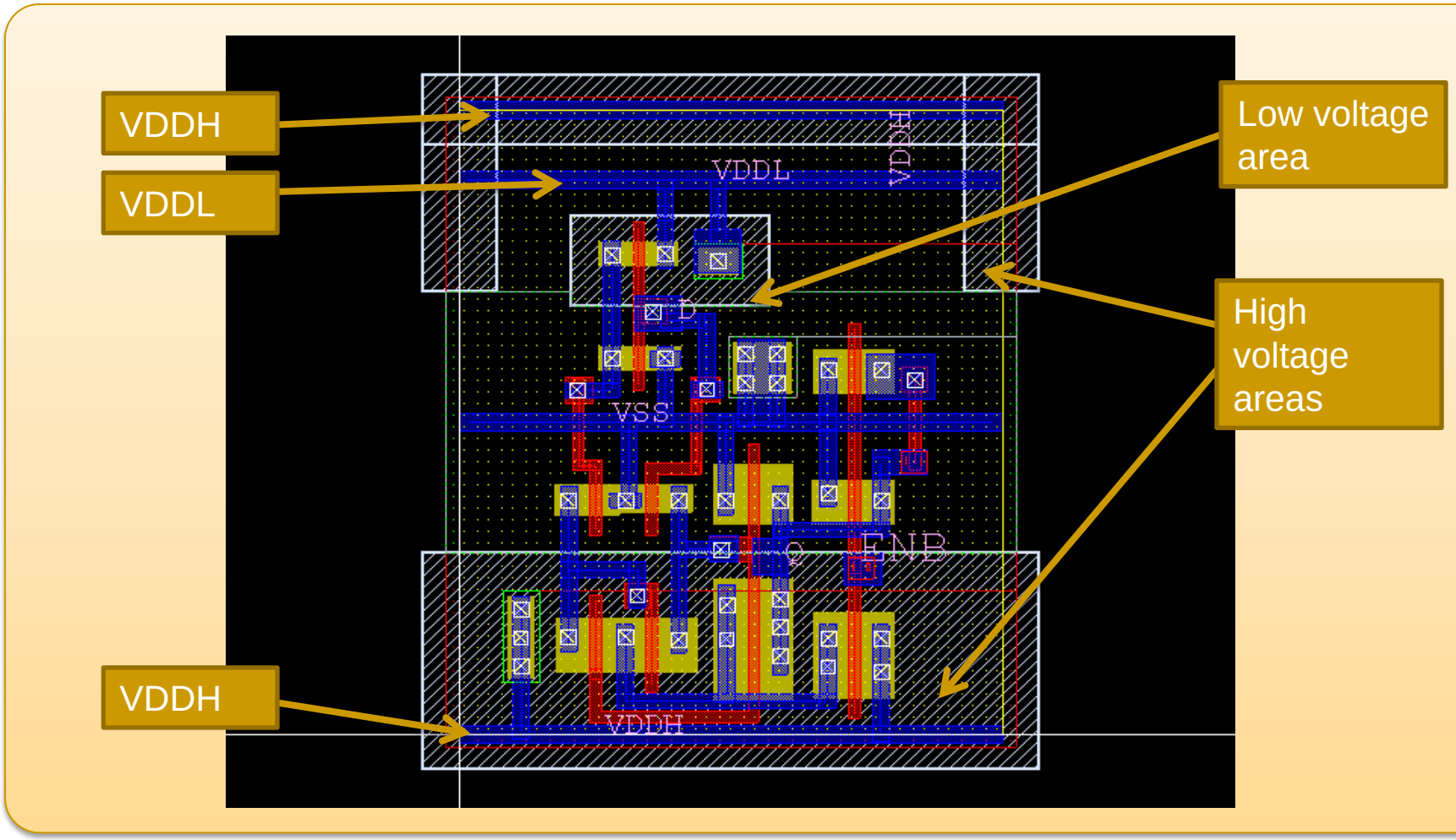
Bypass mode

D(1.2V)	ENB	Q(0.8V)
0	0	0
1	0	1
X	1	1

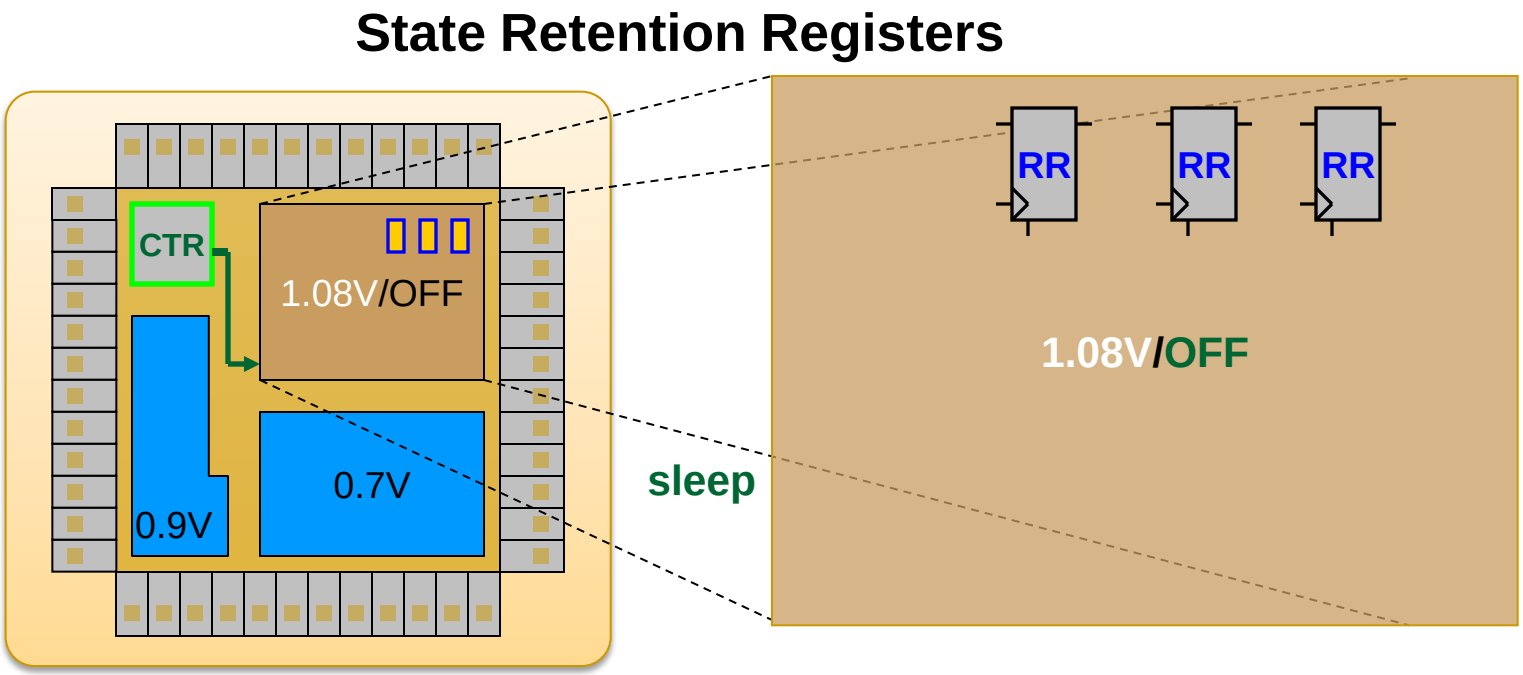
Bypass mode

Output clamped

Enable Level Shifter (low-to-high) Physical design

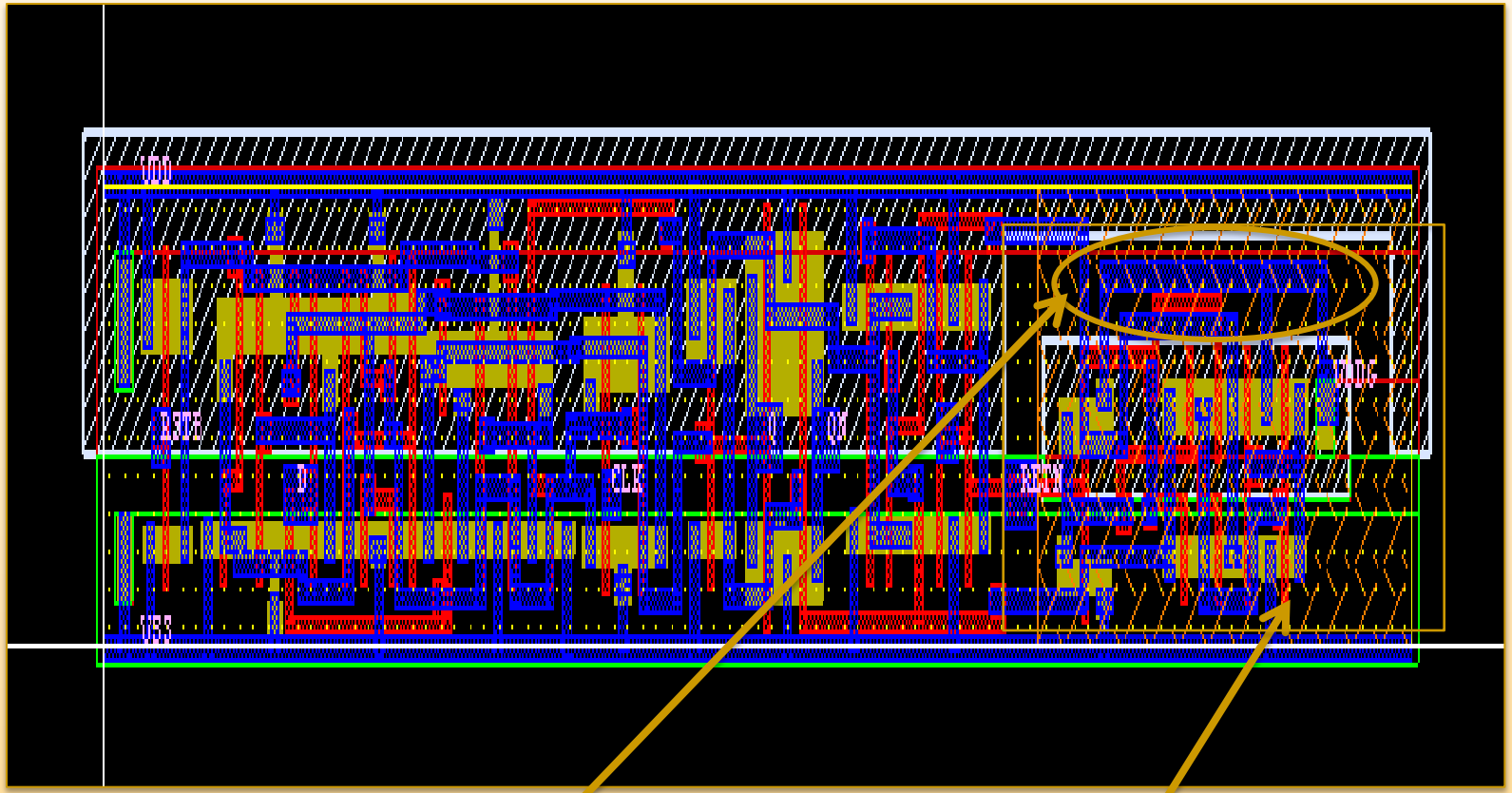


State Retention Registers

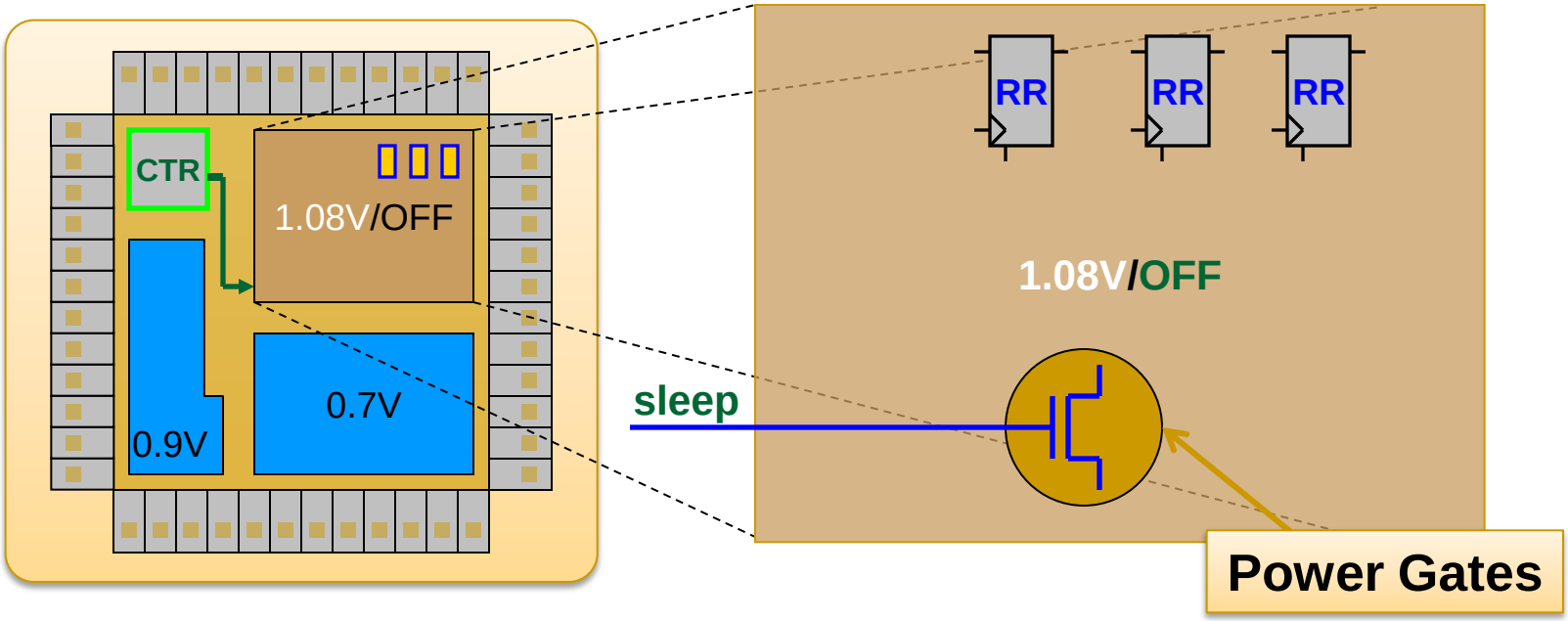


- Retention Register - preserve status while the logic is turned off

Retention Register Physical design

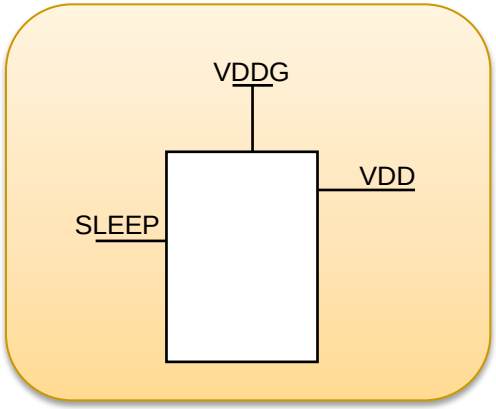


Power Gates

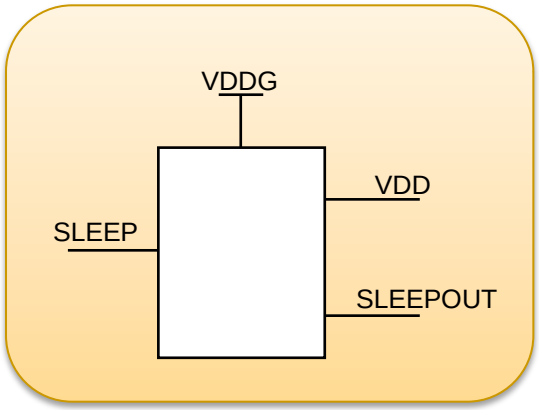


- Retention Register - preserve status while the logic is turned off
- Coarse Grain - Power Gates (switch cells)

Header Cells



Logic Symbol of Header Cell



Logic Symbol of Header Cell(with SLEEPOUT output)

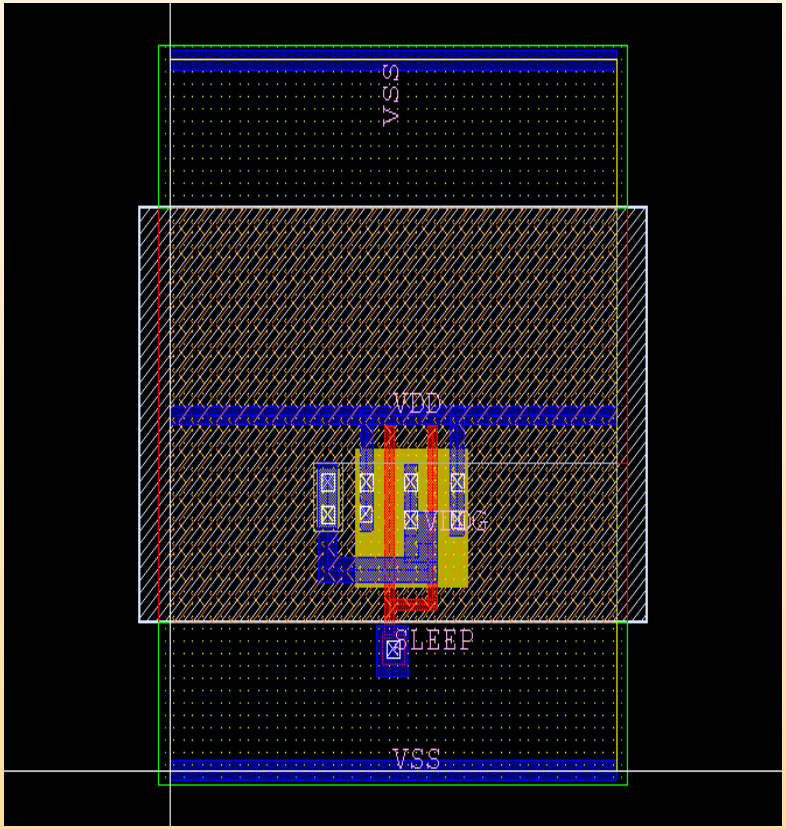
Header Cell Truth Table

SLEEP	VDDG	VDD
0	1	1
1	1	hi-z

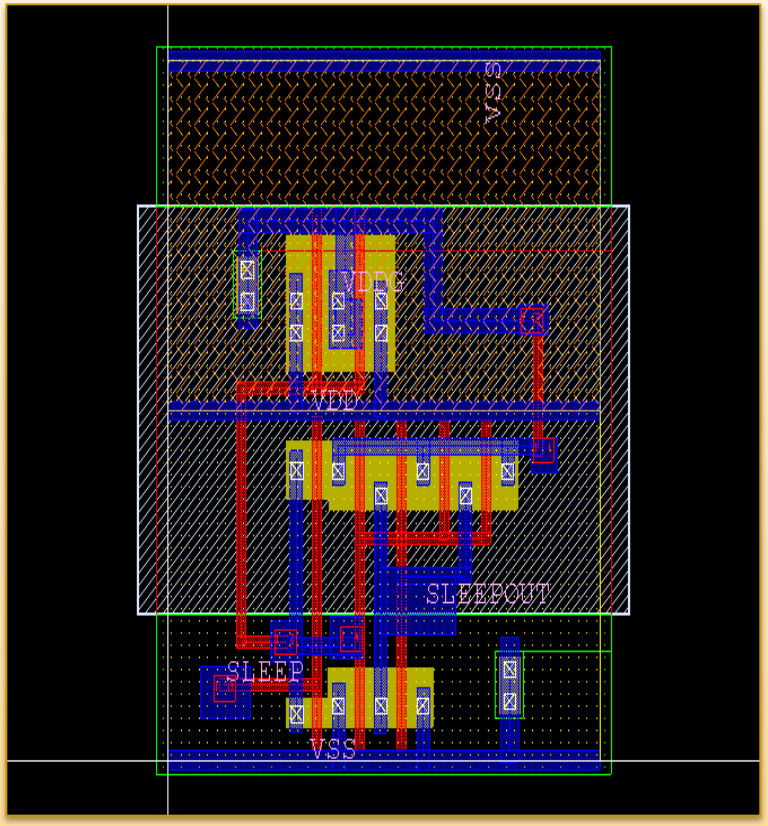
Header Cell (with SLEEPOUT output) Truth Table

SLEEP	VDDG	VDD	SLEEPOUT
0	1	1	0
1	1	hi-z	1

Header Cells Physical Design

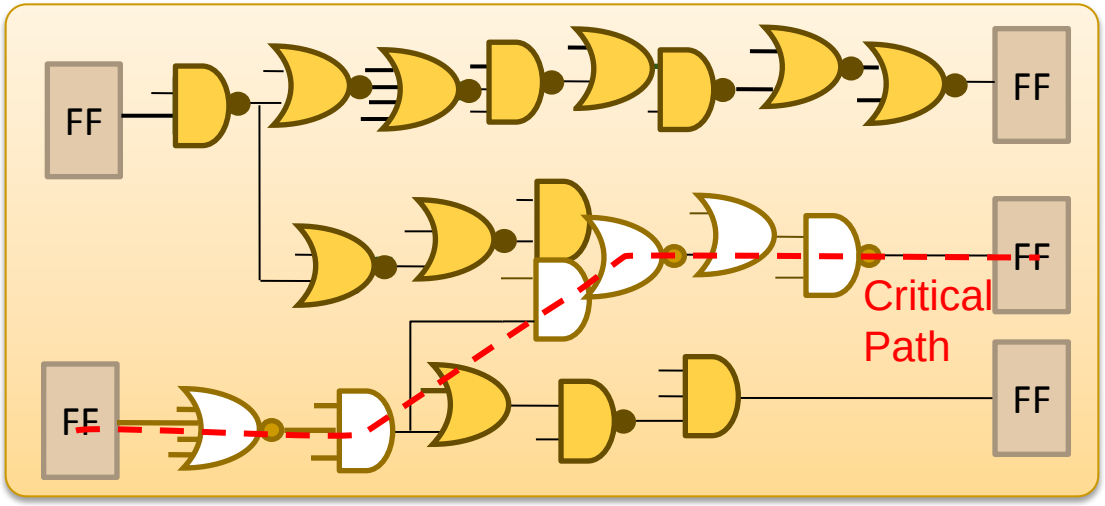


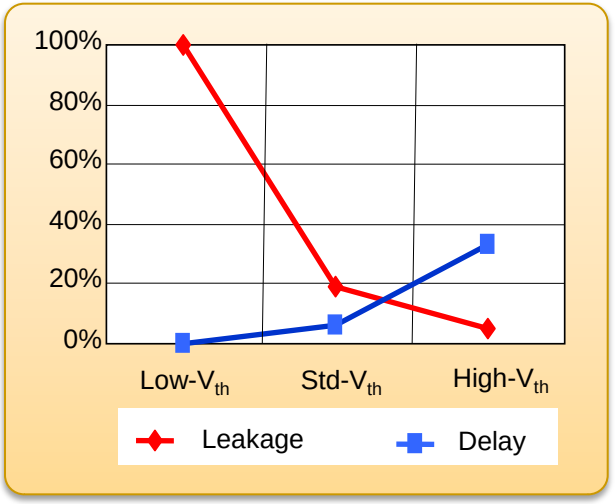
a. Header Cell

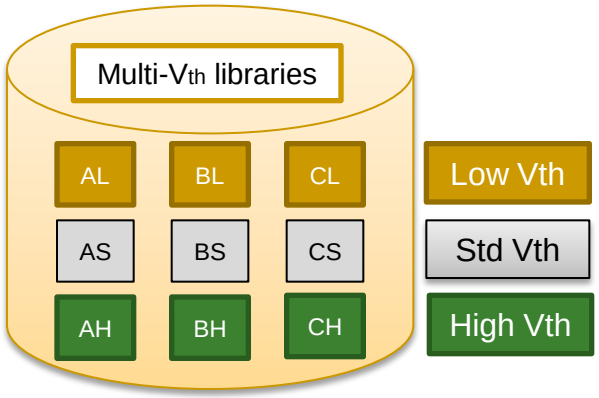


b. Header Cell (with SLEEPOUT output)

Multi-Threshold Libraries





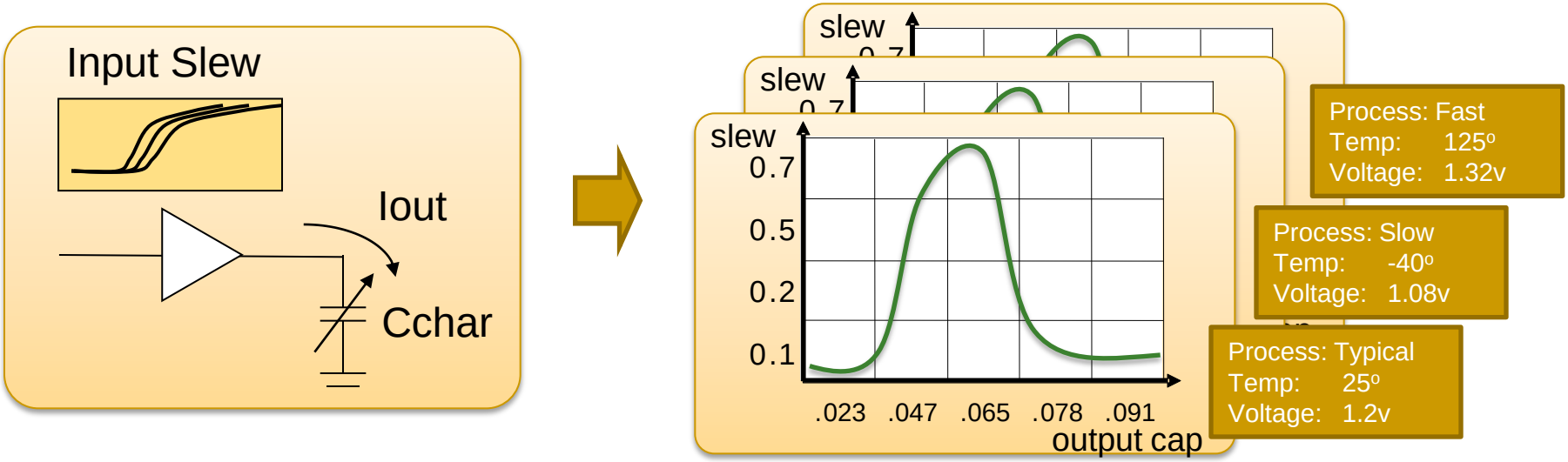


DSCL: Multi Threshold Versions of Cells

- For implementation of Multi-Vth technique the whole DSCL is available in 3 versions (1020 cells)
  - All cells with Low– threshold voltage
  - All cells with Standard – threshold voltage
  - All cells with High– threshold voltage

Characterization

- Characterization computes cell parameter (e.g. delay, output current) depending on input variables: output load, input slew, etc.
- Characterization is preformed for various combinations of operating conditions: process, voltage, temperature (also called PVT corners).



DSCL: Characterization Corners

Corner Name	Process (NMOS proc. – PMOS proc.)	Temperature (T)	Power Supply (V)	Notes
TTNT1p20v	Typical - Typical	25	1.2	Typical corner
SSHT1p08v	Slow - Slow	125	1.08	Slow corner
FFLT1p32v	Fast - Fast	-40	1.32	Fast corner
FFHT1p32v	Fast - Fast	125	1.32	High leakage corner
SSLT1p32v	Slow - Slow	-40	1.32	Low temperature corners
SSLT1p08v	Slow - Slow	-40	1.08	
Low Voltage Operating Conditions				
TTNT0p80v	Typical - Typical	25	0.80	Typical corner
SSHT0p70v	Slow - Slow	125	0.70	Slow corner
FFLT0p90v	Fast - Fast	-40	0.90	Fast corner
FFHT0p90v	Fast - Fast	125	0.90	High leakage corner
SSLT0p90v	Slow - Slow	-40	0.90	Low temperature corners
SSLT0p70v	Slow - Slow	-40	0.70	

DSCL: Additional Data

- Power / ground (PG) pin definitions are required for all cells in a library
  - Defined as attributes in .lib
  - Allows accurate definition of multiple power / ground pin information
- Benefits
  - Power domain driven synthesis
  - Automatic power net connections
  - PST-based optimization
  - Verification of PG netlist vs. power domains
  - Power switch verification

```
pg_pin(VDD) {
   std_cell_main_rail : true ;
   voltage_name : VDD;
   pg_type      : primary_power;
 }
 pg_pin(VSS) {
   voltage_name : VSS;
   pg_type      : primary_ground;
 }
```

DSCL: Power Verilog Models

- Power Verilog models
  - Separate verilog models with power modeling

```
module AND2X1 (IN1,IN2,Q,VDD,VSS);
output  Q;
input   IN1,IN2;
inout   VDD;
inout   VSS;
power_down  iQ (Q, Qint, VDD, VSS);

and  (Qint,IN1,IN2);
endmodule
```

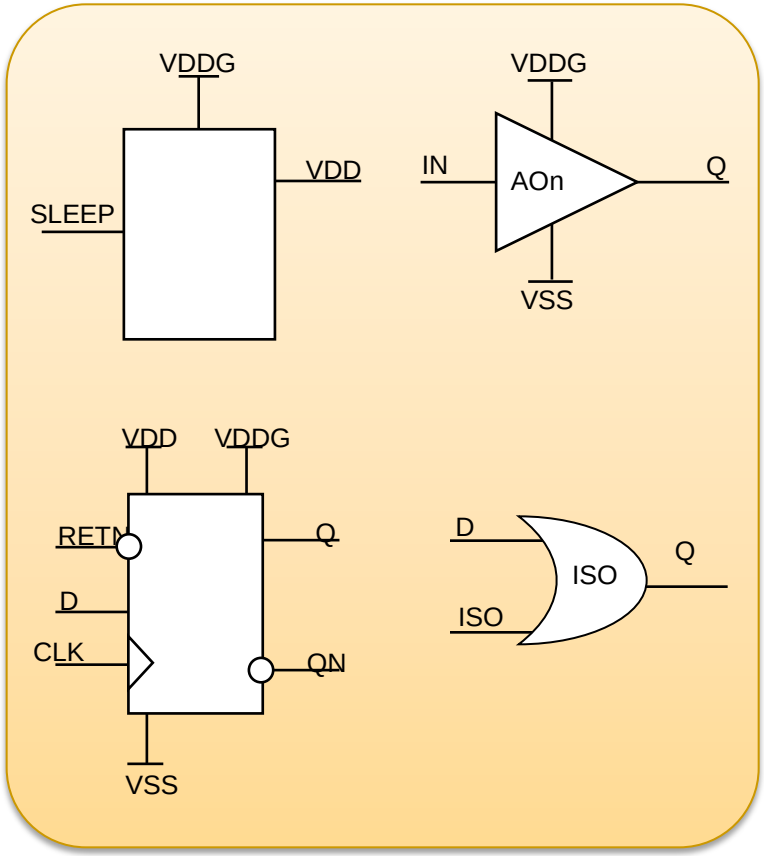
Modeling output state dependence on power

```
module AND2X1(IN1,IN2,Q);
output  Q;
input   IN1,IN2;

and (Q,IN2,IN1);

endmodule
```

```
primitive power_down  (Q, Qint, vdd, vss);
  output Q;
  input  Qint, vdd, vss;
  table
    0   1   0 : 0 ;
    1   1   0 : 1 ;
    ?   0   0 : x ;
    ?   0   1 : x ;
    ?   1   1 : x ;
    ?   x   ? : x ;
    ?   ?   x : x ;
  endtable
endprimitive
```

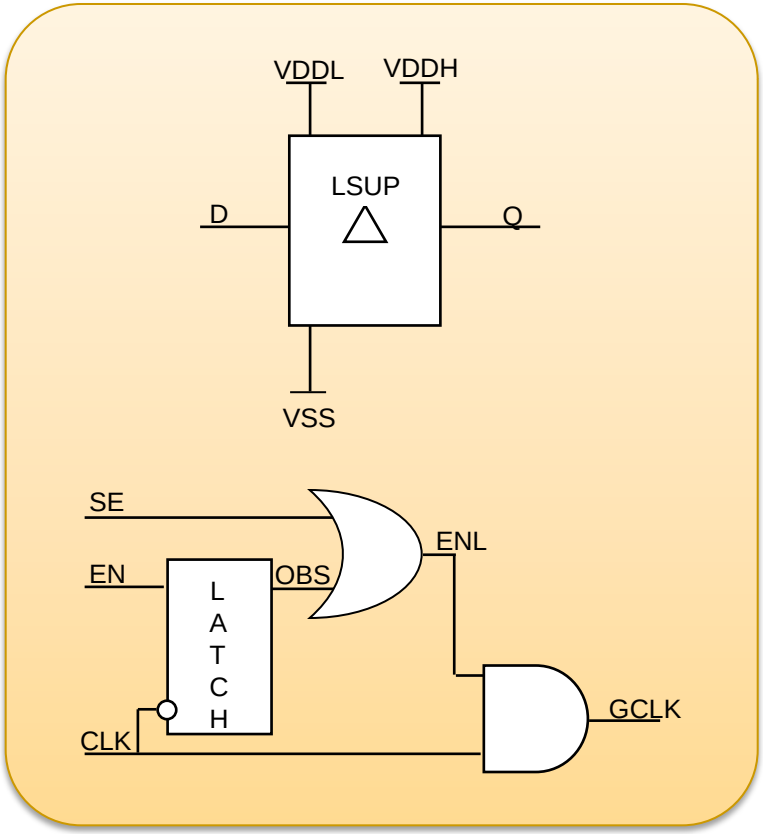
DSCL: Special Cells for Low Power Techniques (1)

- Power Gatings
  - 5 cells with different loads
- Always on
  - 10 cells: 3 inverters, 3 buffers and 4 DFFs
- Retention cells
  - 44 cells negedge/posedge, scan
- Isolation cells
  - 8 cells with different logic, load

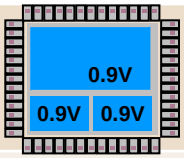
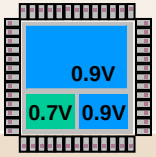
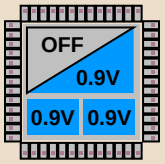
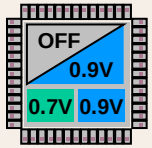
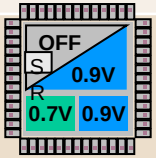


DSCL: Special Cells for Low Power Techniques (2)

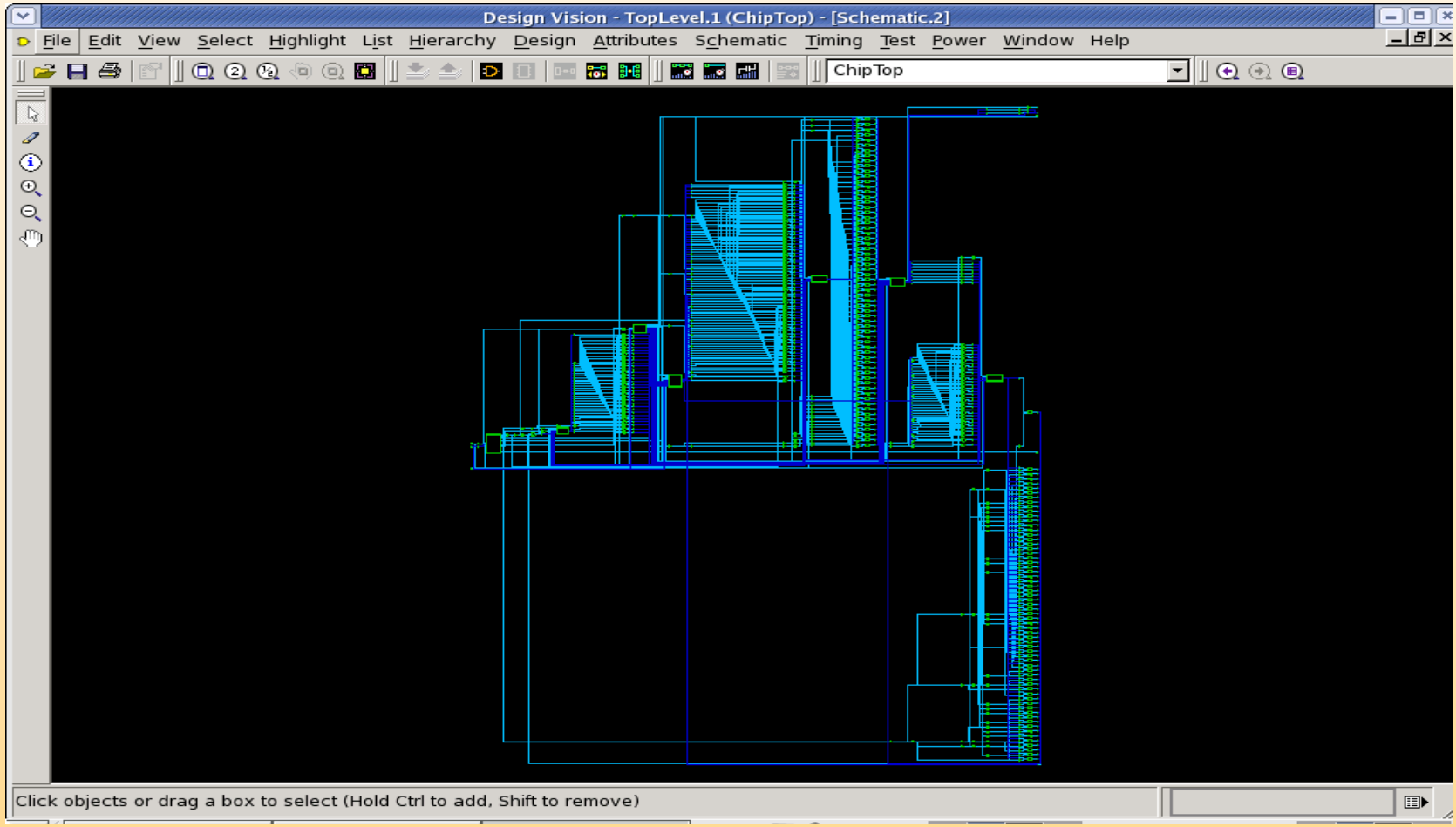
- Level shifters
  - 16 cells Low/High, High/Low, with or without enable, with different loads
- Clock gatings:
  - 11 cells with different loads, edges, and control (post/pre)
- HVT Cells
  - All logical cells are designed using HVT, LVT



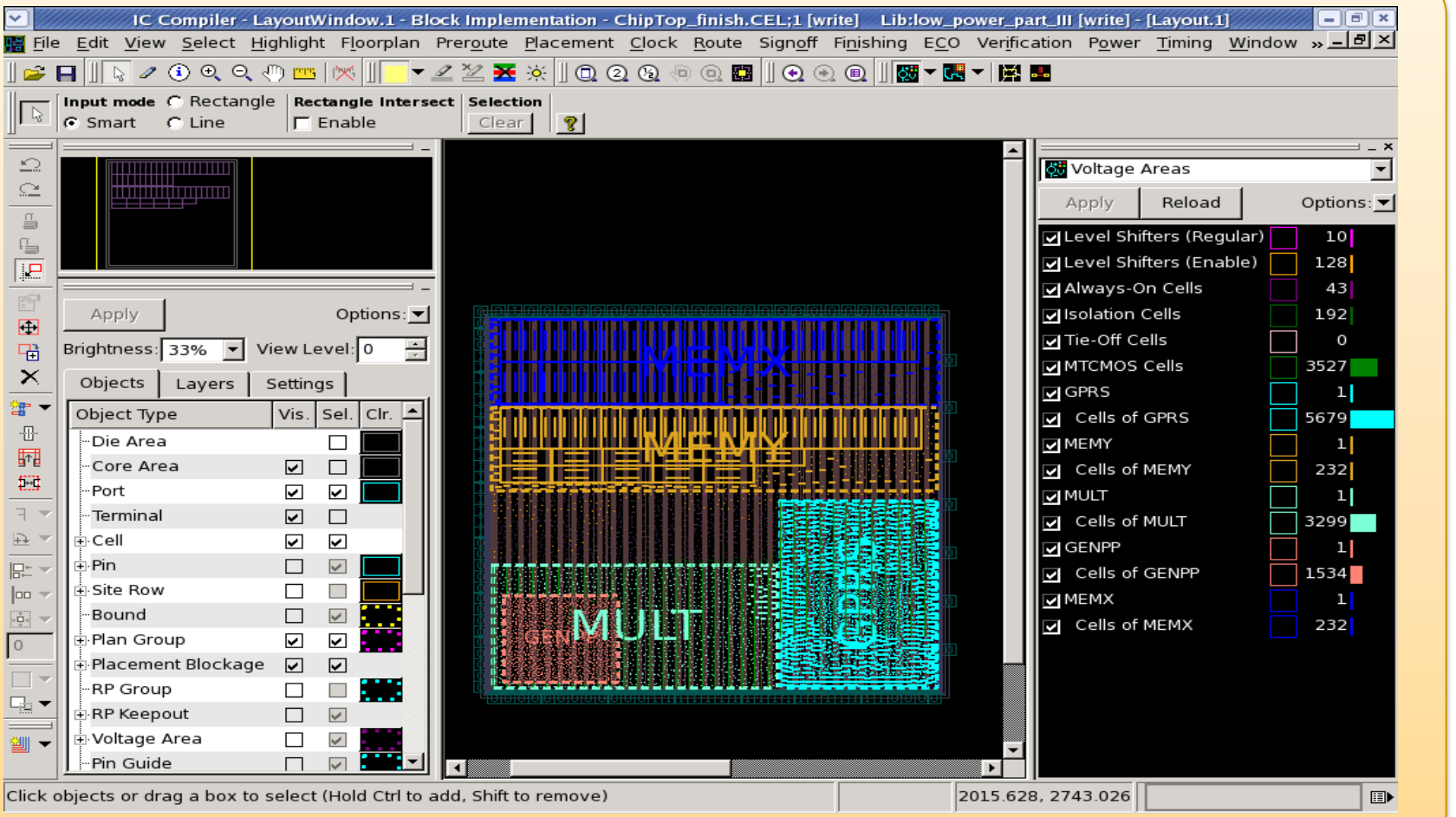
DSCL: Special Cells for Low Power Techniques (3)

		Power Gates (MTCMOS)	Isolation Cells	Level Shifters	Retention Registers	Always On Logic
	Multiple Power Domains Single Voltage					
	Multiple Voltage (MV) Domains			+		
	Power Gating (shut down) Single Voltage No State Retention	+	+			+
	MV Domains Power Gating No State Retention	+	+	+		+
	MV Domains Power Gating State Retention	+	+	+	+	+

Low Power Design of ChipTop Developed with DSCL: DC view



Low Power Design of ChipTop Developed with DSCL: ICC View



Conclusion

- Low Power Design requires significant design flow modifications
  - UPF enables LPD flow automation
- Low Power design techniques have their huge impact on libraries
- SAED 90nm EDK DSCL includes all special cells needed for low power design techniques
- This 90nm EDK is currently in use in 235 universities of 37 countries
- This 90nm EDK is used inside Synopsys for education of customers

- Currently similar EDK is being developed for 32/28nm technology, initial release is planned in June 2011