Extended Applications of Current Source Modeling [1]

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[1] Based on “Accurate Timing and Noise Analysis of Combinational and Sequential Logic Cells Using Current Source Modeling” by Shahin Nazarian, Hanif Fatemi and Massoud Pedram

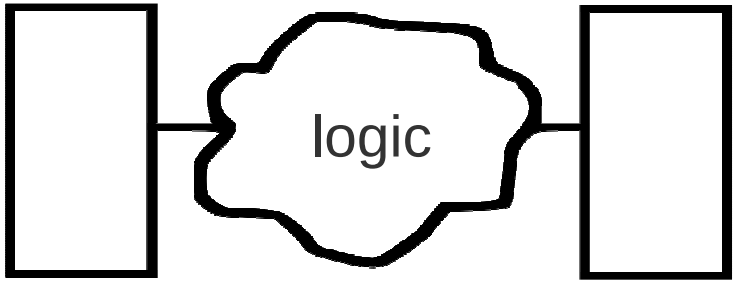
Outline

- Motivation
- Basics
  - MOSFET - Transistor model
  - Capacitive cross-talk noise
- Blade/Razor
- Combinatorial Model
  - Inverter
  - Transmission Gate

- Sequential Model (CMOS Latch)
  - Transparent Mode
  - Opaque Mode
  - Complete Model

- Summary

Motivation



- Feature sizes getting smaller (layout geometries < 65 nm)
- Increasing packing density and frequency
- Increasing effect of analog effects

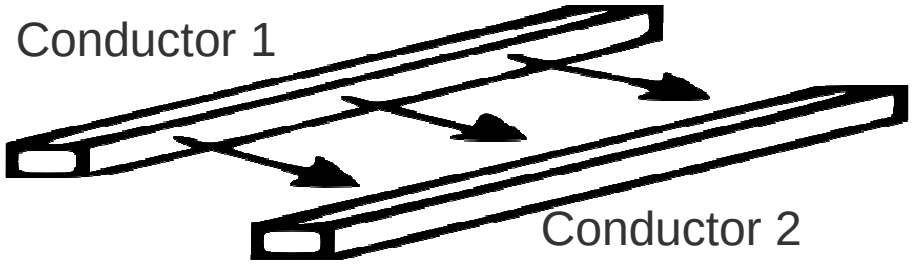
→ Need for an accurate model to do timing analysis

→ Current Source Model ←

Capacitive Crosstalk Noise

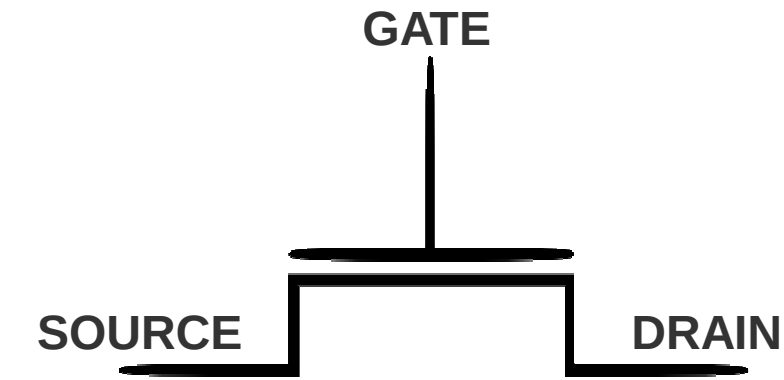
- Interconnection of logic cells
- Analog effects are regarded as noise (“capacitive crosstalk noise”)
- Different input voltage waveforms influence the delay of the cells

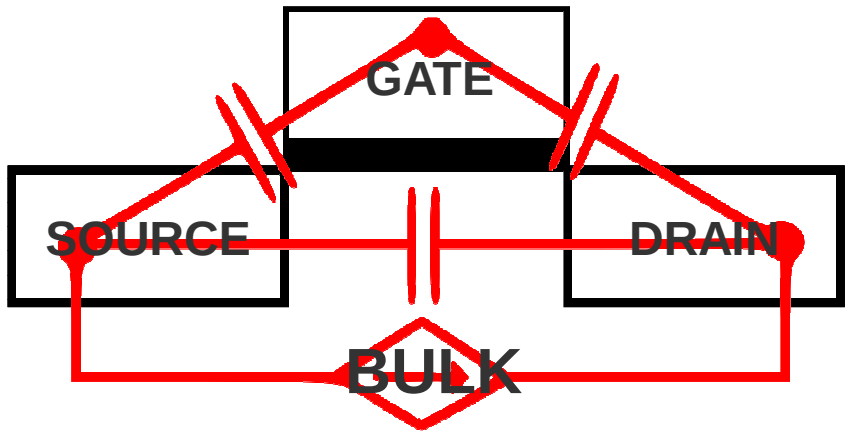
  → The model has to be able to deal with any noisy input voltage waveform and with any arbitrary load



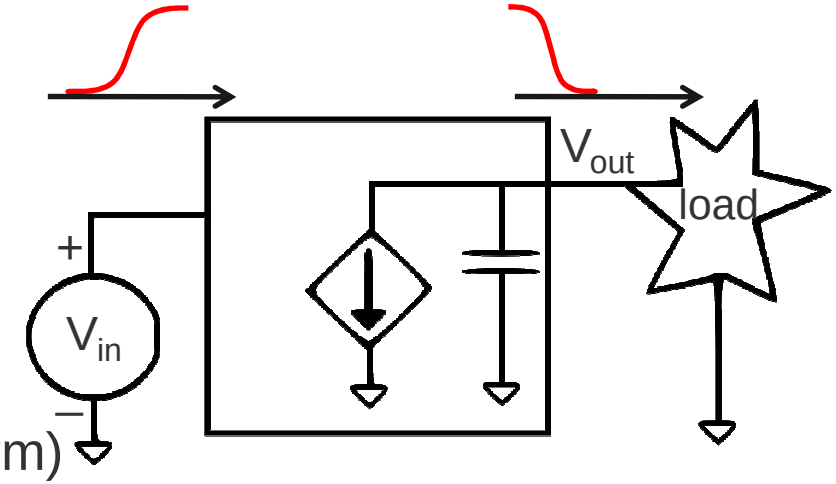
Transistor Model

- Basis for all Current Source Models
- Used to derive Combinational/Sequential Models
- Interconnection of NMOS/PMOS Transistors and simplification





Blade/Razor[2]



- Blade = Current Source Model
- Razor = interconnect model
  (algorithm to calculate output waveform)

→ First model that can deal with arbitrary Input/Output Voltage and arbitrary loads

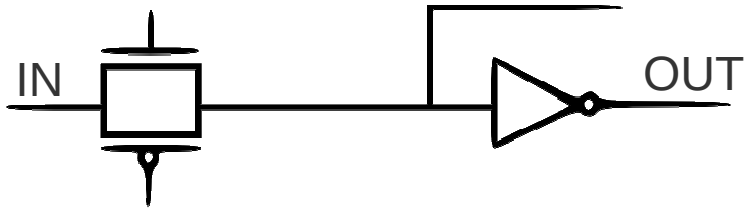
→ Voltage Controlled Current Source, internal capacitance and input waveform timeshift

[2] As introduced in “Blade and Razor: Cell and Interconnect Delay Analysis Using Current-Based Models” by John Croix and D.F.Wong

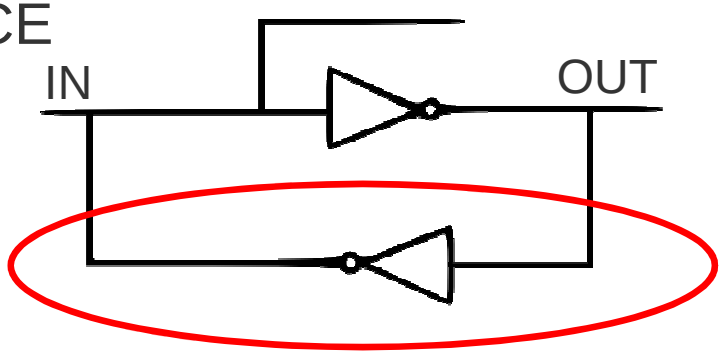
Combinatorial Model

- For any CMOS logic cell
- No feedback loops (output only dependent on input)
- Calculate output to an arbitrary input voltage

  combinatorial
- Result almost as accurate as SPICE

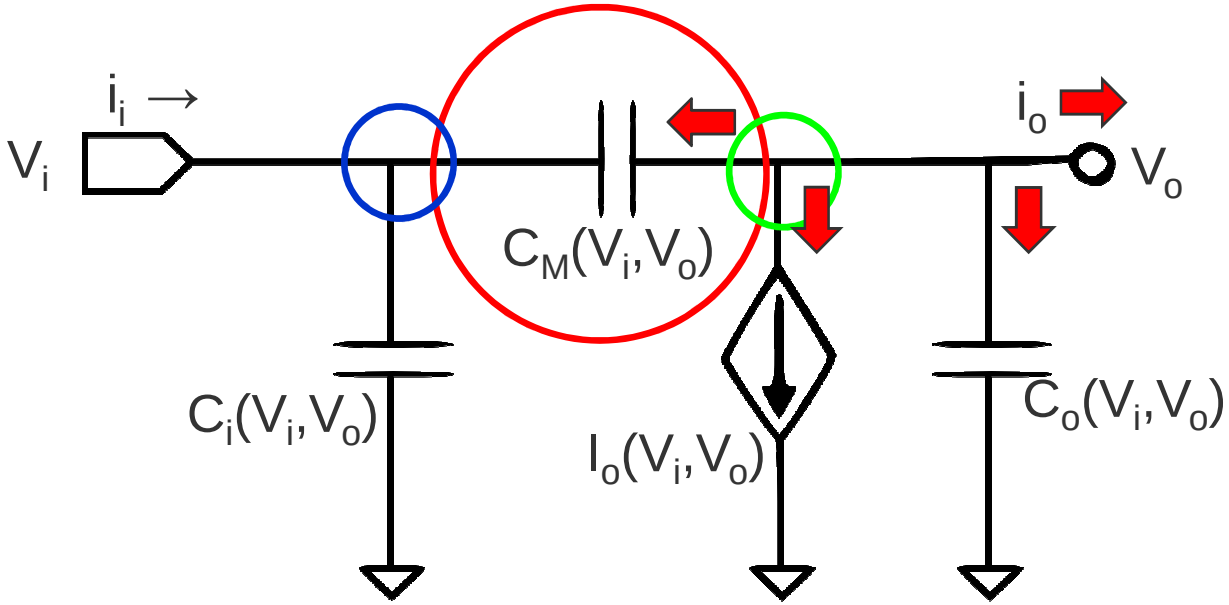


sequential



Inverter

Main Difference to existing CSMs: Capturing parasitic effects between input and output node!



Equations for the current:

(I1) $$i_o + I_o(V_i,V_o) + \left(C_o(V_i,V_o) + C_M(V_i,V_o)\right)\frac{dV_o}{dt} - C_M(V_i,V_o)\frac{dV_i}{dt} = 0$$

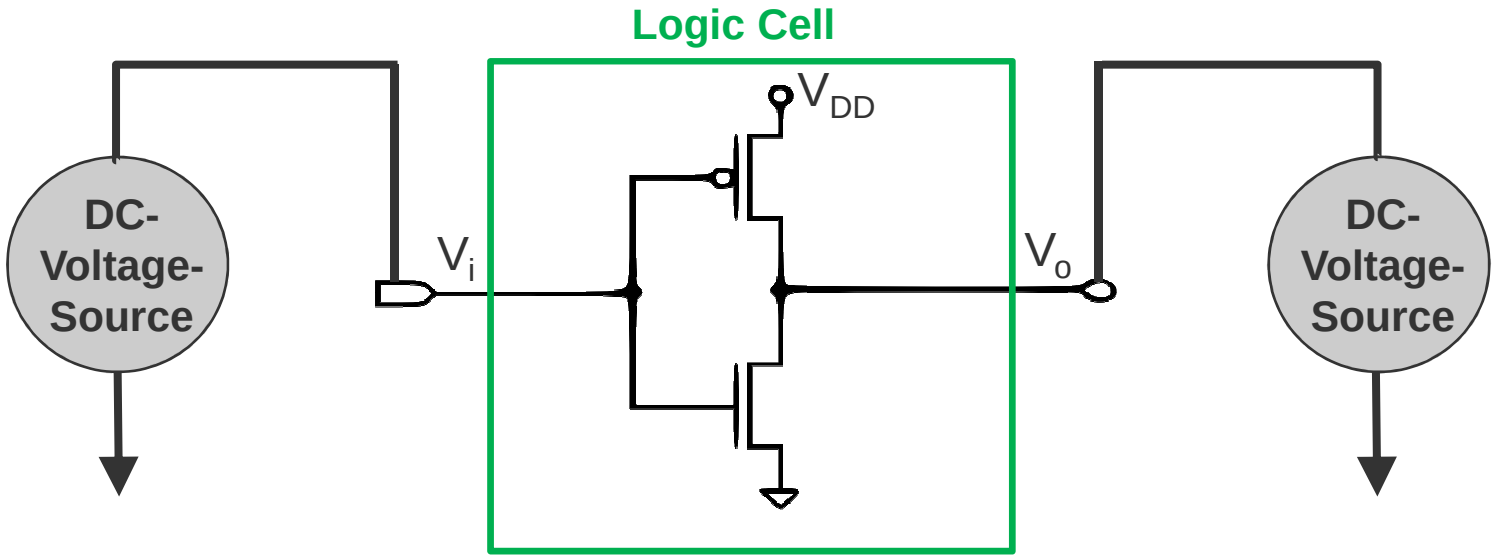
(I2) $$i_i - \left(C_i(V_i,V_o) + C_M(V_i,V_o)\right)\frac{dV_i}{dt} + C_M(V_i,V_o)\frac{dV_o}{dt} = 0$$

Characterization of I_o

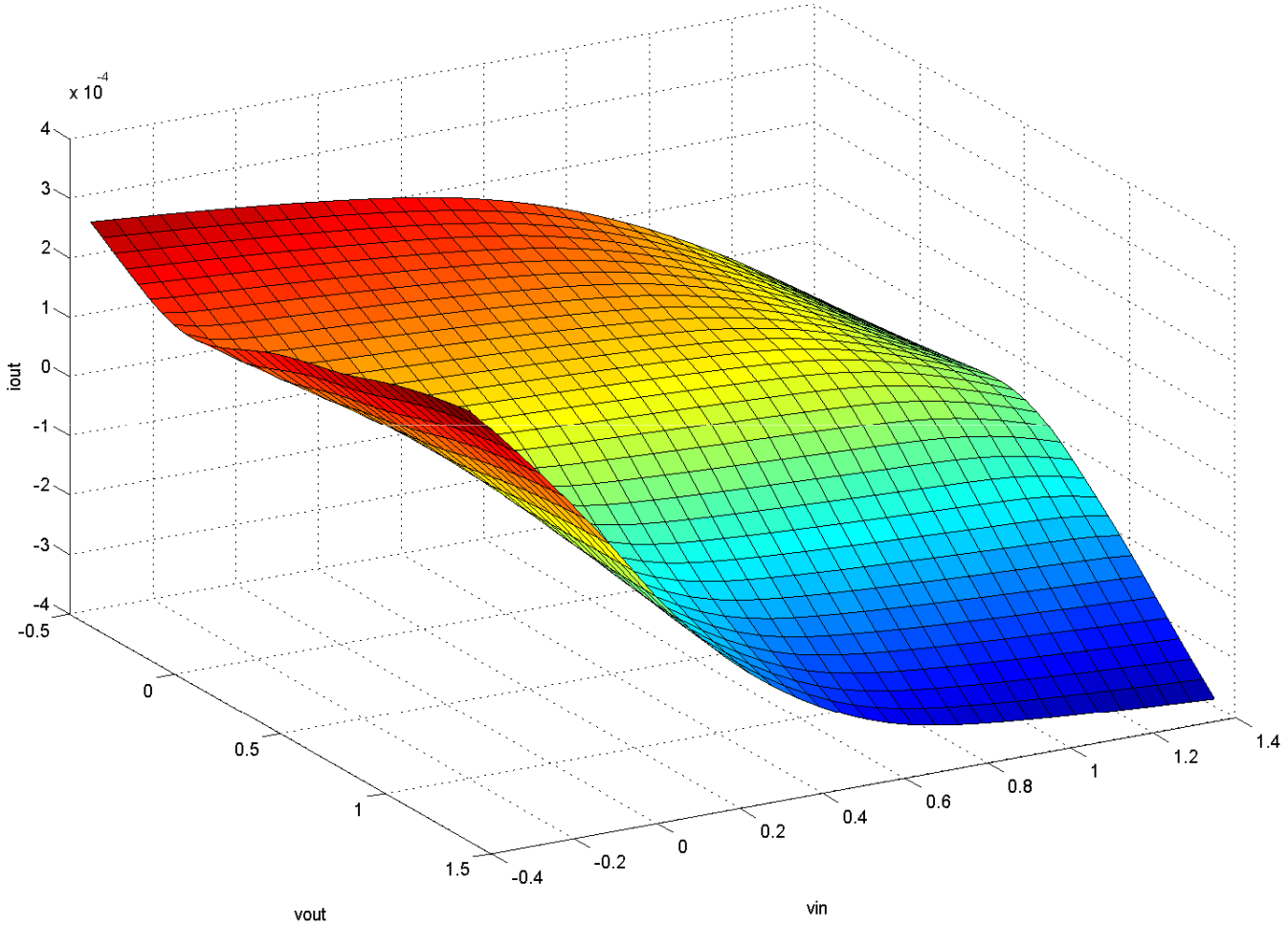
- Connect dc-voltage source to V_i and V_o (swept from $-\Delta$ to $V_{DD}+\Delta$)

$$(\mathrm{I1})\; i_o + I_o(V_i, V_o) + \left(C_o(V_i, V_o) + C_M(V_i, V_o)\right)\frac{dV_o}{dt} - C_M(V_i, V_o)\frac{dV_i}{dt} = 0$$

- Measure i_o to get value of $I_o(V_i,V_o)$



Characteristic Values of the Current Source

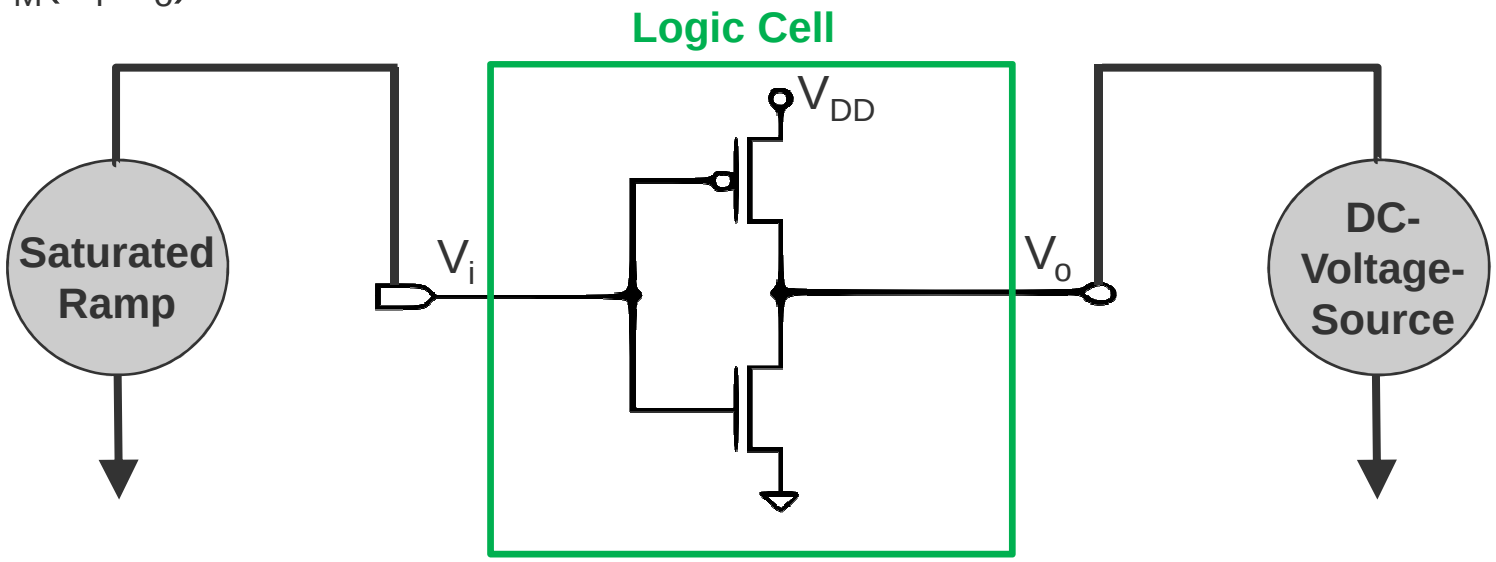


Characterization of C_M

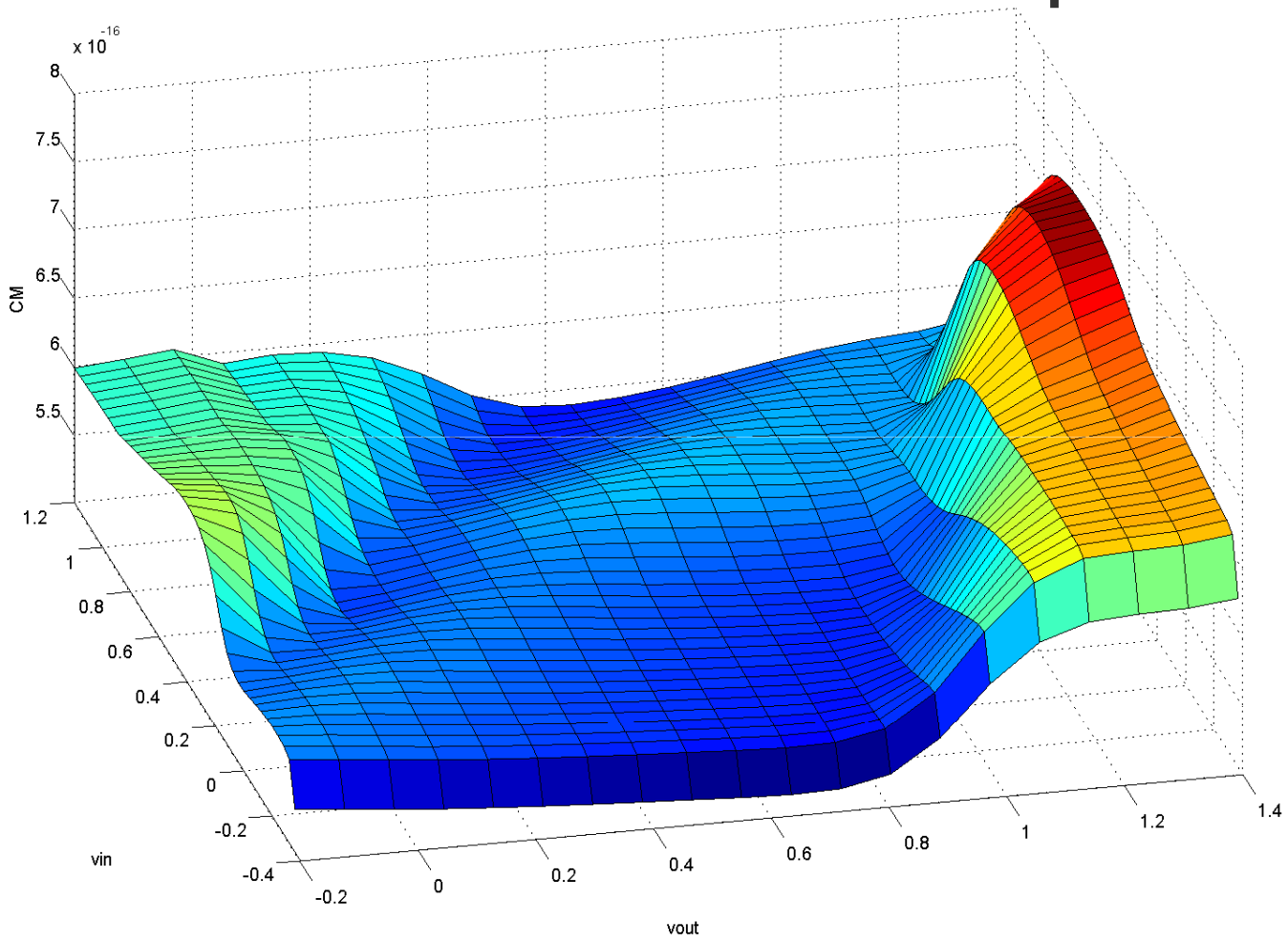
- Connect dc-voltage source to V_o (swept from $-\Delta$ to $V_{DD}+\Delta$)
- Connect V_i to a saturated ramp

$$(\mathrm{I1})\; i_o + I_o(V_i, V_o) + \cancel{\left(C_o(V_i, V_o) + C_M(V_i, V_o)\right)\frac{dV_o}{dt}} - C_M(V_i, V_o)\frac{dV_i}{dt} = 0$$

- Measure i_o (I_o already characterized) to calculate the value of $C_M(V_i,V_o)$



Characteristic Values of the Miller Capacitance

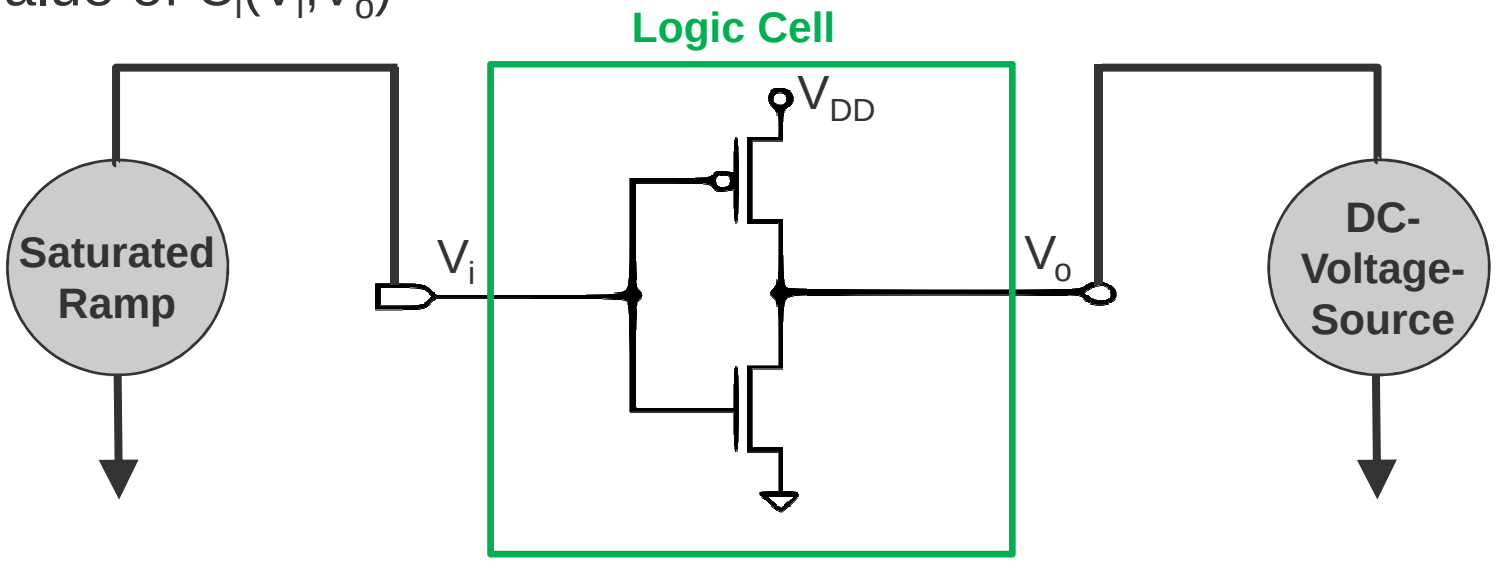


Characterization of C_i

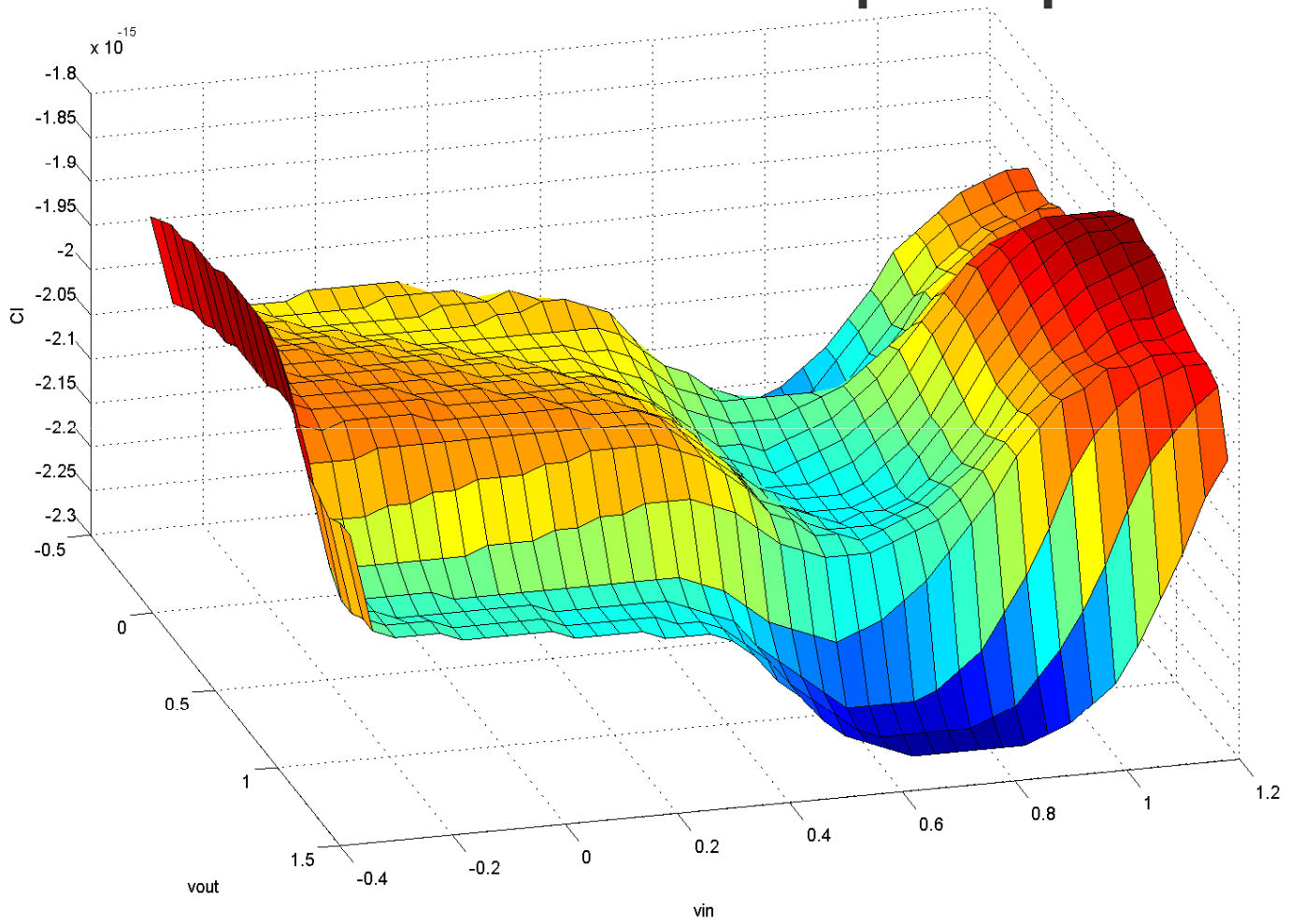
- Connect dc-voltage source to V_o (swept from $-\Delta$ to $V_{DD}+\Delta$)
- Connect V_i to a saturated ramp

$$(\mathrm{I2})\; i_i - \left(C_i(V_i,V_o) + C_M(V_i,V_o)\right)\frac{dV_i}{dt} + \cancel{C_M(V_i,V_o)\frac{dV_o}{dt}} = 0$$

- Measure i_i (I_o and C_M already characterized) to calculate the value of $C_i(V_i,V_o)$



Characteristic Values of the Input Capacitance

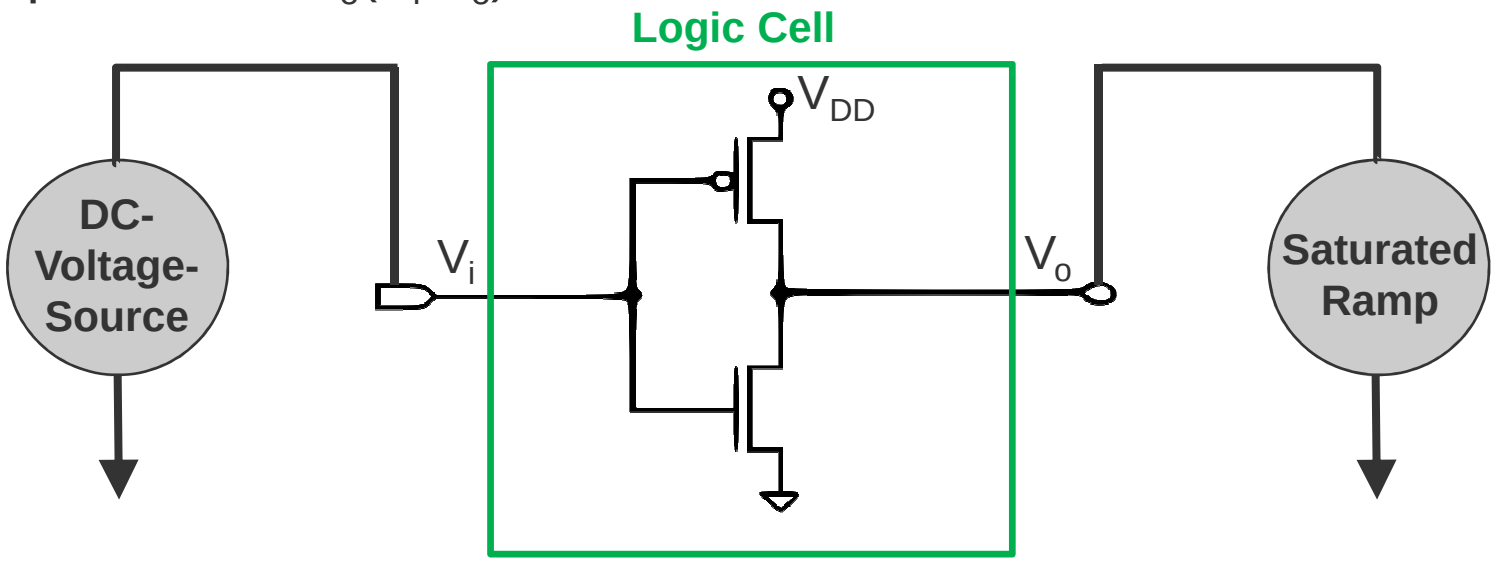


Characterization of C_O

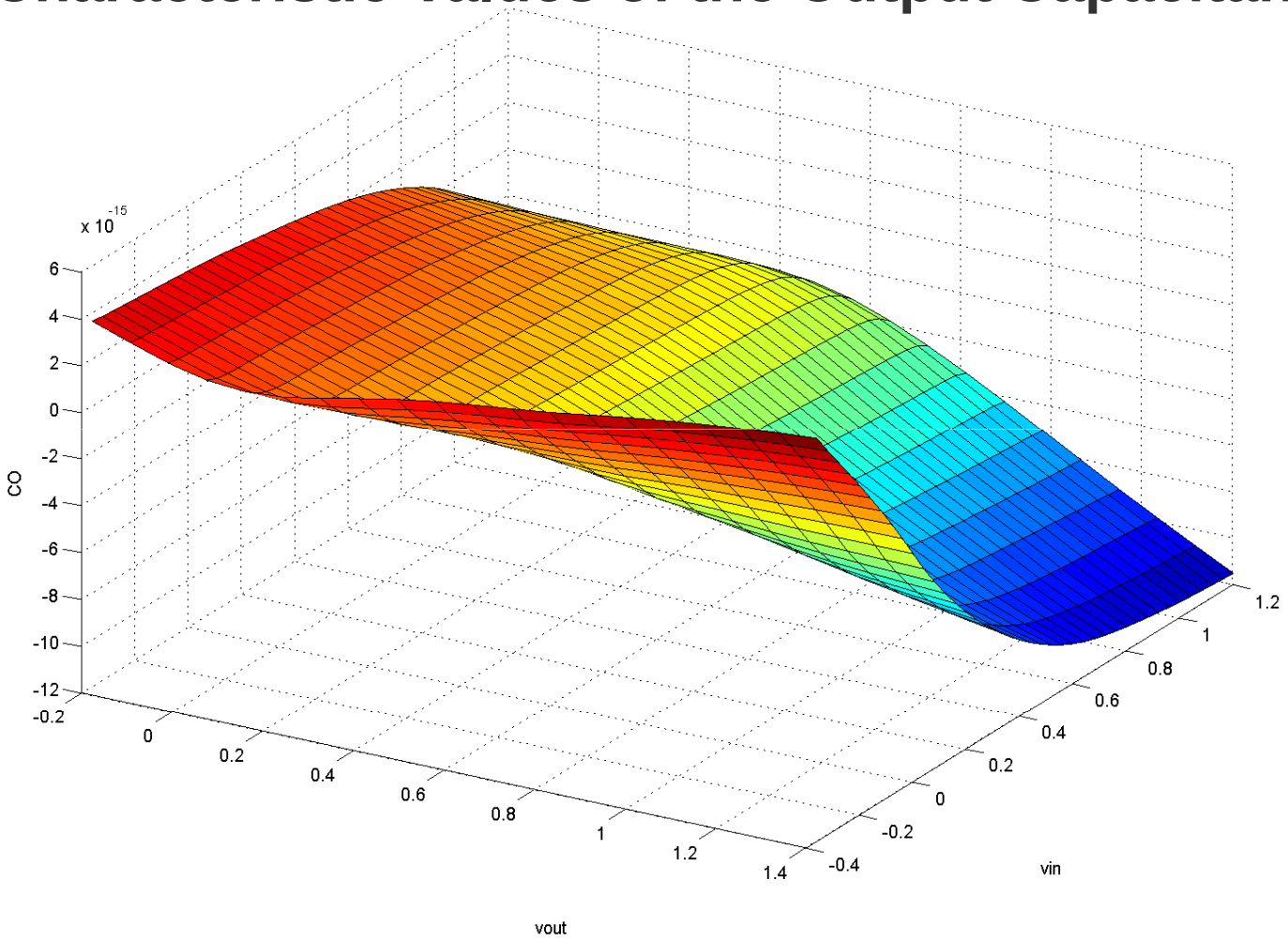
- V_i connected to dc-voltage, V_o connected to a saturated ramp)

$$(\mathrm{I1})\; i_o + I_o(V_i,V_o) + \left(C_o(V_i,V_o) + C_M(V_i,V_o)\right)\frac{dV_o}{dt} - \cancel{C_M(V_i,V_o)\frac{dV_i}{dt}} = 0$$

- Measure i_o (I_o and C_M already characterized) and solve equation for $C_o(V_i,V_o)$



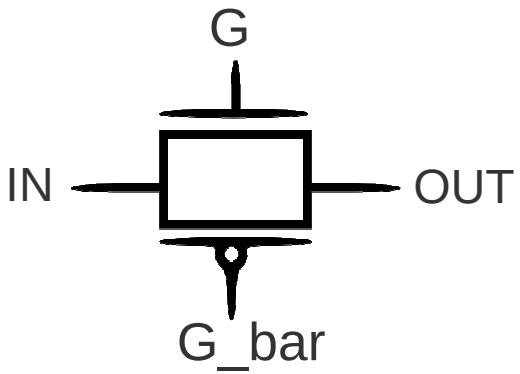
Characteristic Values of the Output Capacitance

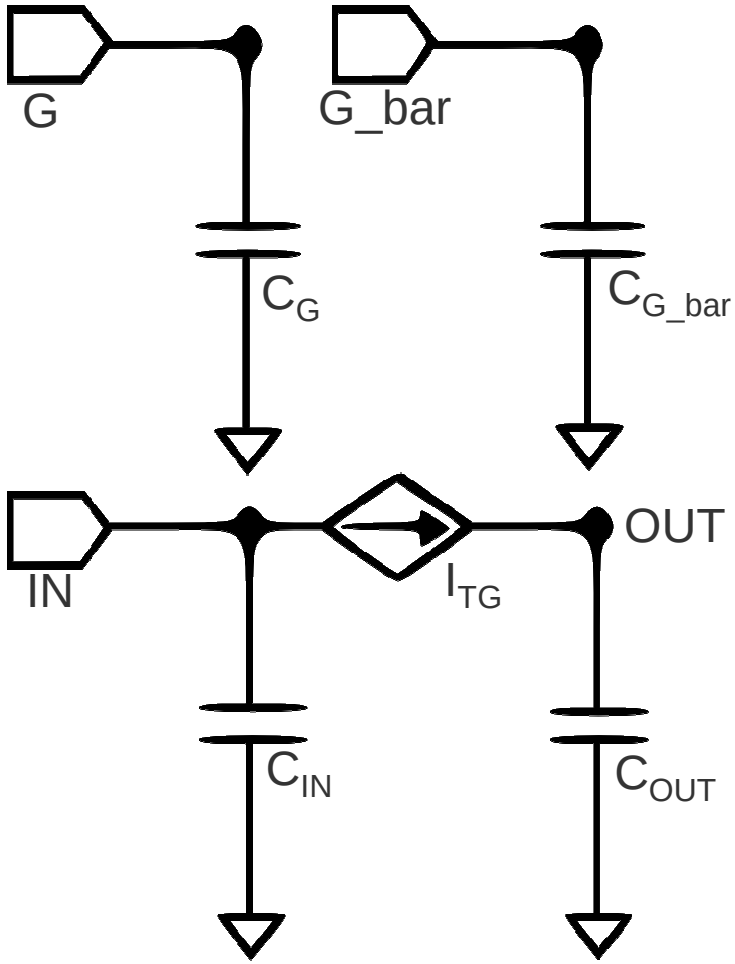


Transmission Gate

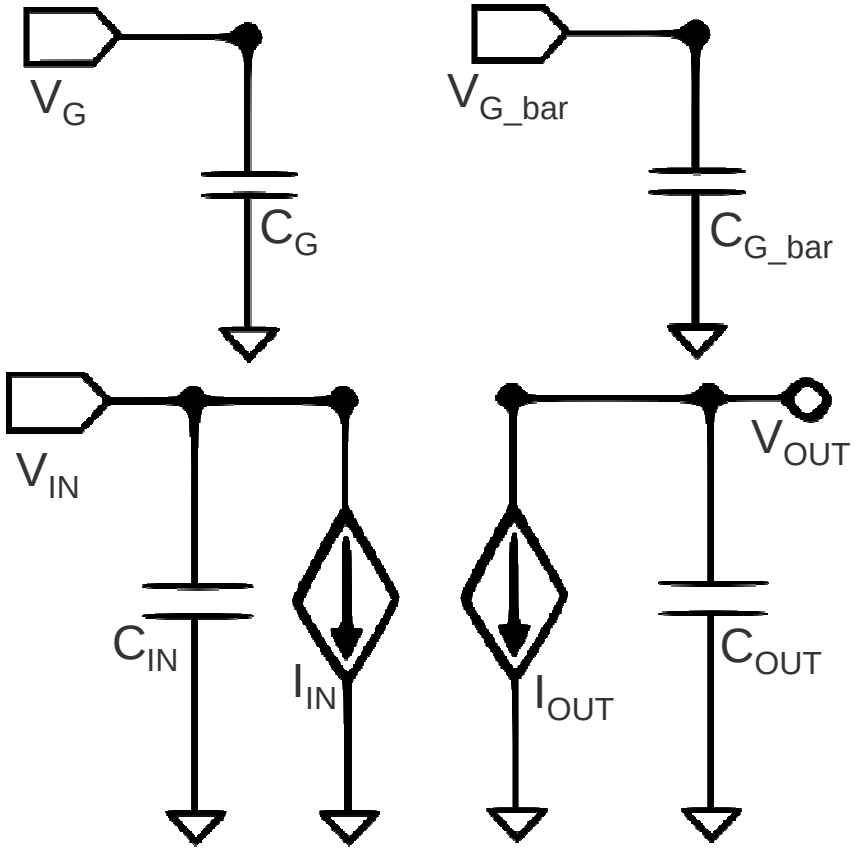
3 Cases:

- OFF
- Conducting (OUT = IN)
- Rising/Falling Transition





CSM for the Transmission Gate



Components:

$$C_G = C_G(V_{IN},V_{OUT},V_G)$$
$$C_{G\_bar} = C_{G\_bar}(V_{IN},V_{OUT},V_{G\_bar})$$

$$C_{IN} = C_{IN\text{-}G}(V_{IN},V_{OUT},V_G) + C_{IN\text{-}G\_bar}(V_{IN},V_{OUT},V_{G\_bar})$$

$$C_{OUT} = C_{OUT\text{-}G}(V_{IN},V_{OUT},V_G) + C_{OUT\text{-}G\_bar}(V_{IN},V_{OUT},V_{G\_bar})$$

$$I_{IN} = I_{IN\text{-}G}(V_{IN},V_{OUT},V_G) + I_{IN\text{-}G\_bar}(V_{IN},V_{OUT},V_{G\_bar})$$

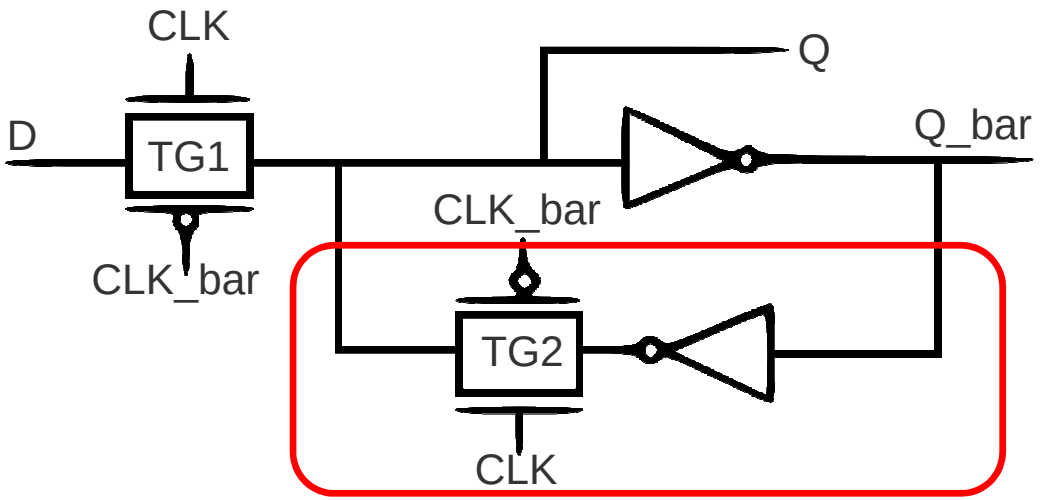
I_{TG} and I_{OUT} analog

Sequential Model

- Combination of combinatorial models

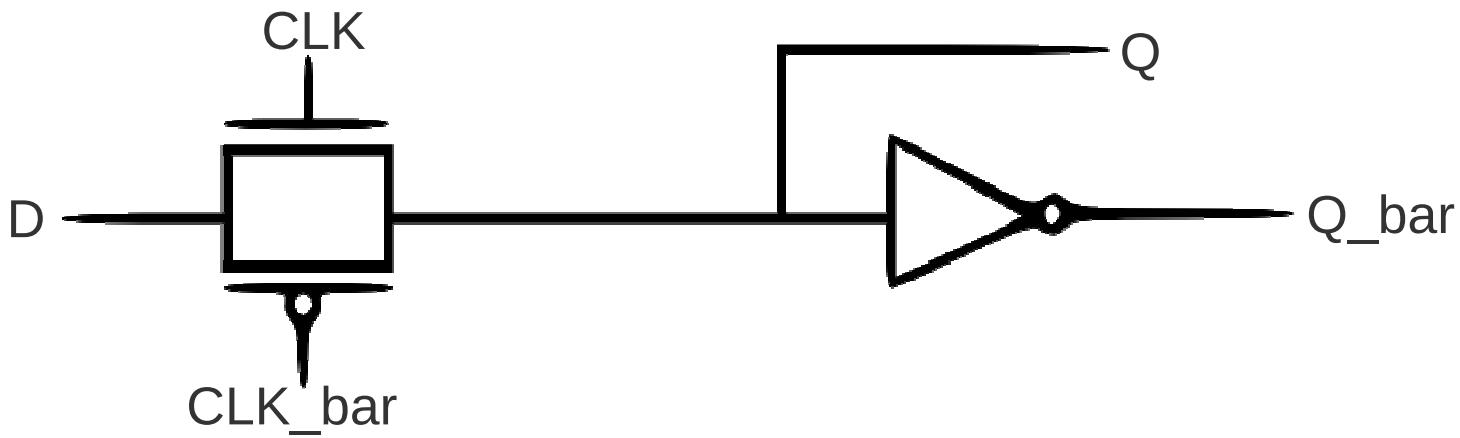
- Feedback loops
  ⟶ noise can be magnified

- Example: Latch (3 possible modes)
  - Transparent
  - Opaque
  - Transition

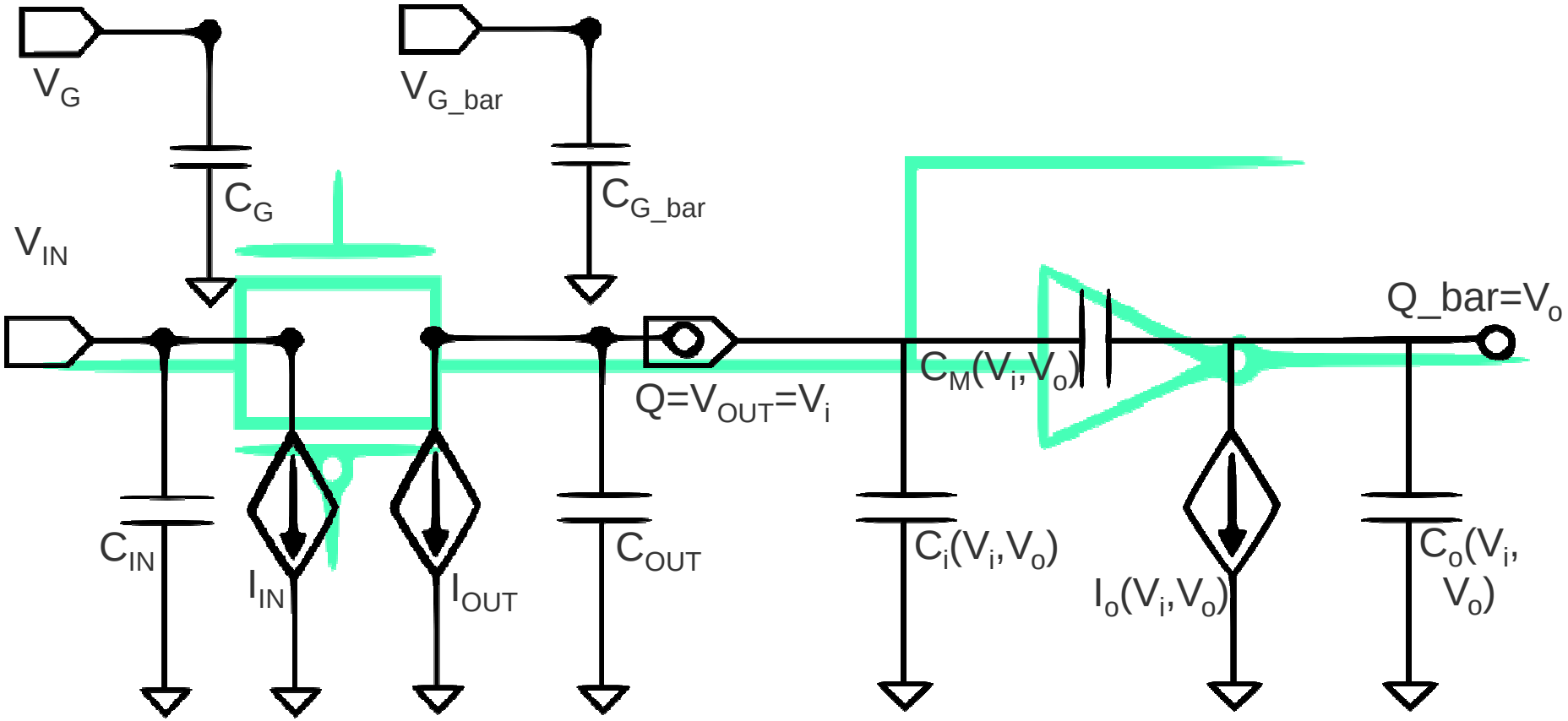


Transparent Mode

- CLK = 1
- TG1 conducts and TG2 is off
- No feedback loop
- Q = D

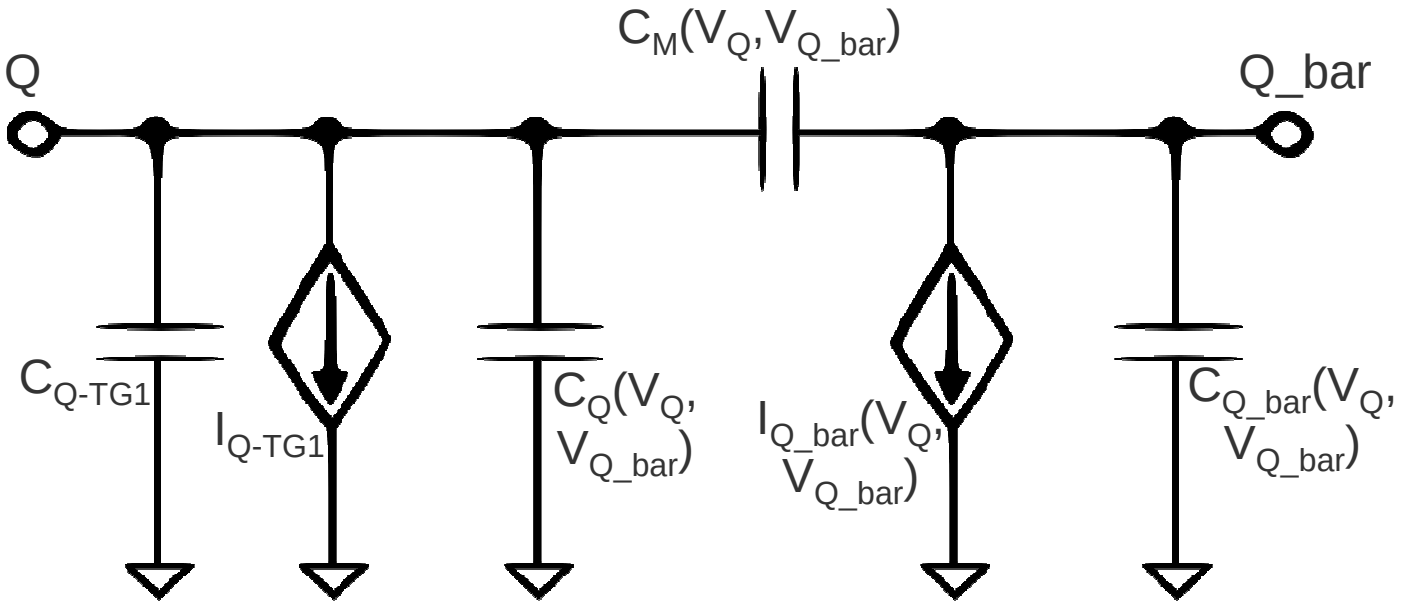


Derivation of the CSM



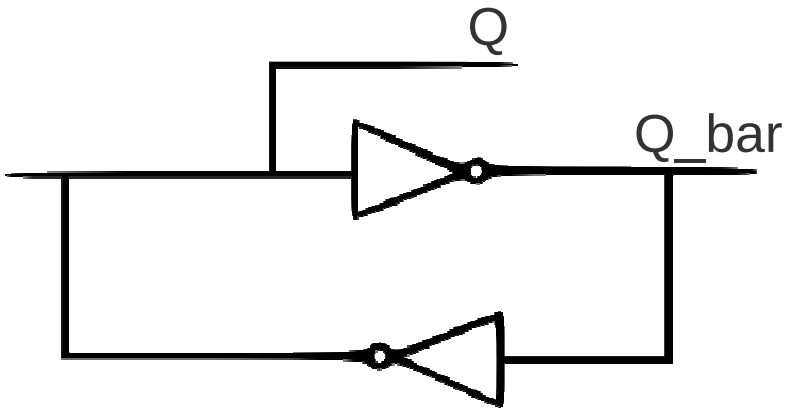
CSM for Latch in Transparent Mode

$$I_{Q\text{-}TG1} = I_{Q\text{-}CLK\_bar}(V_D, V_Q, V_{CLK\_bar}) + I_{Q\text{-}CLK}(V_D, V_Q, V_{CLK})$$
$$C_{Q\text{-}TG1} = C_{Q\text{-}CLK\_bar}(V_D, V_Q, V_{CLK\_bar}) + C_{Q\text{-}CLK}(V_D, V_Q, V_{CLK})$$

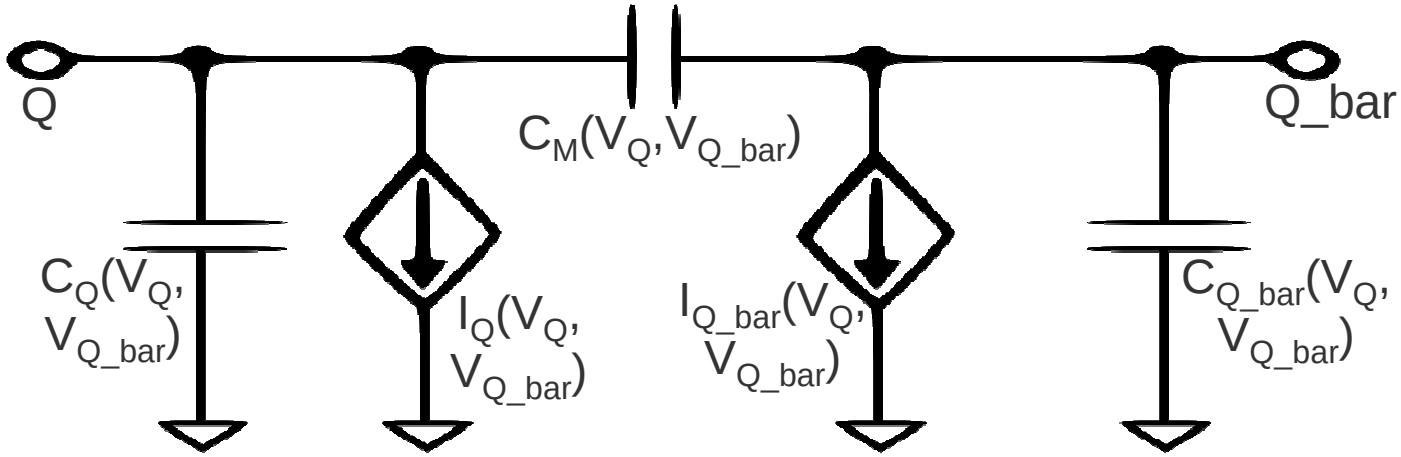


Opaque Mode

- CLK = 0
- TG2 conducts and TG1 is off
- Disconnected input data D
- Q and Q_bar stabilize each other



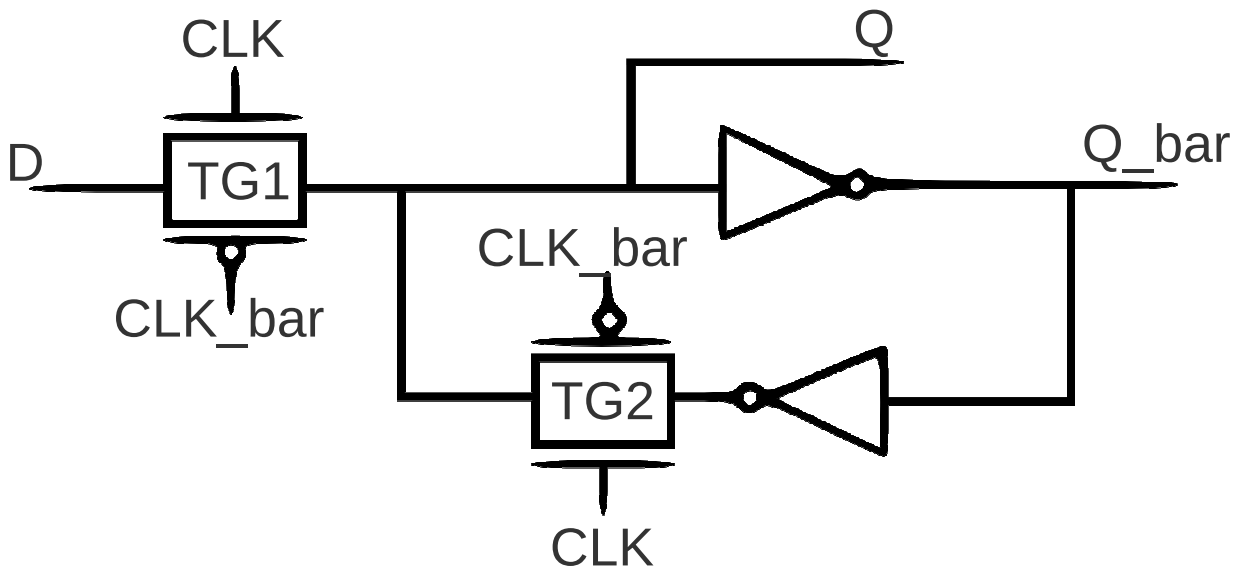
CSM for Latch in Opaque Mode



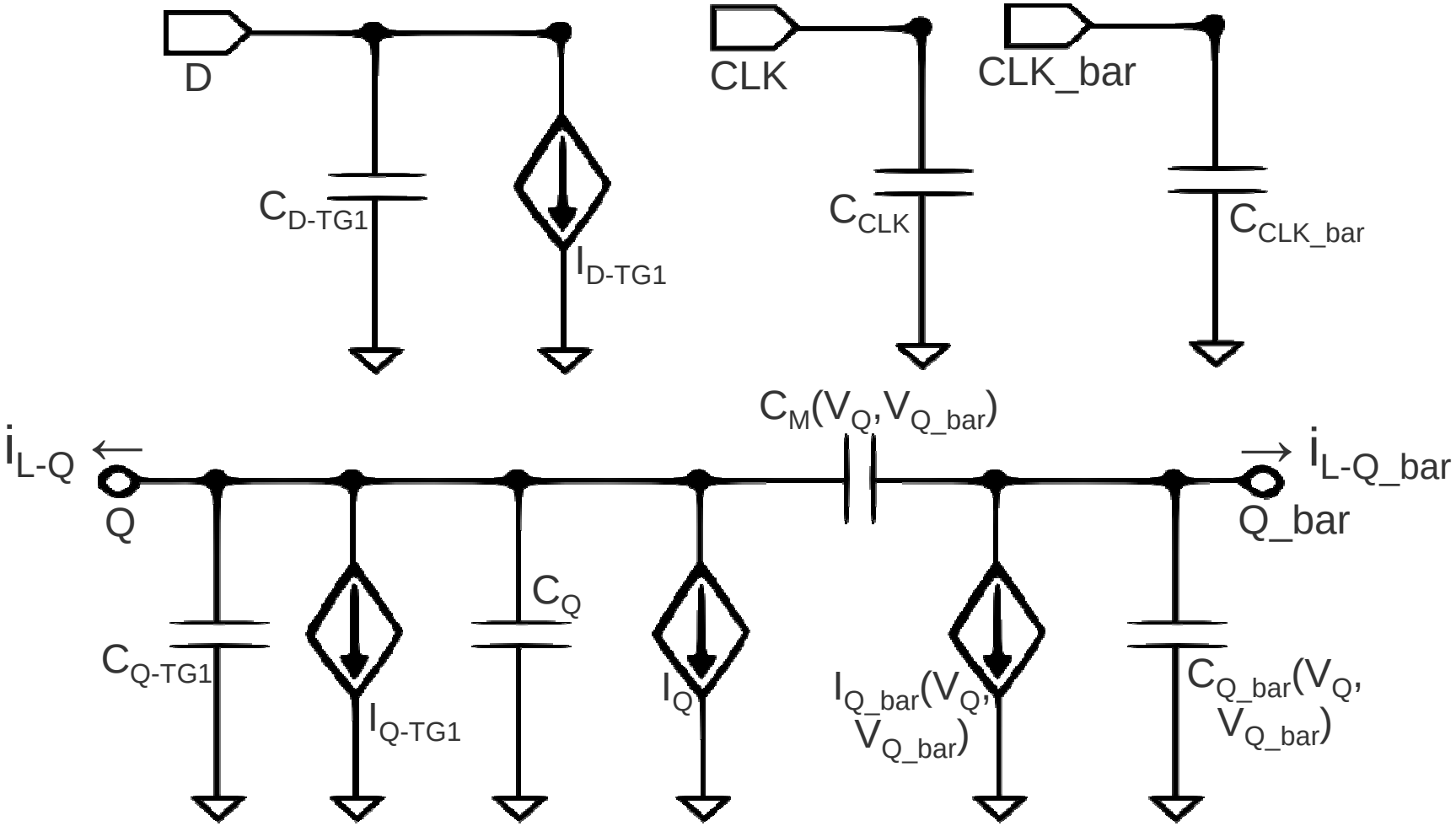
Transition Mode

- CLK in Transition (rising or falling slope)
- Both TGs partially conducting
- All components influence output

→ same CSM as complete model for the latch



Complete Model



Summary

- New Current Source Model for Combinational Logic Cells
- Derivation of a model for Sequential Logic Cells
- Possibility of modeling noise effects
- Possibility of accurately calculating the output voltage to any arbitrarily shaped input voltage

BACKUP

Output Calculation (Inverter)

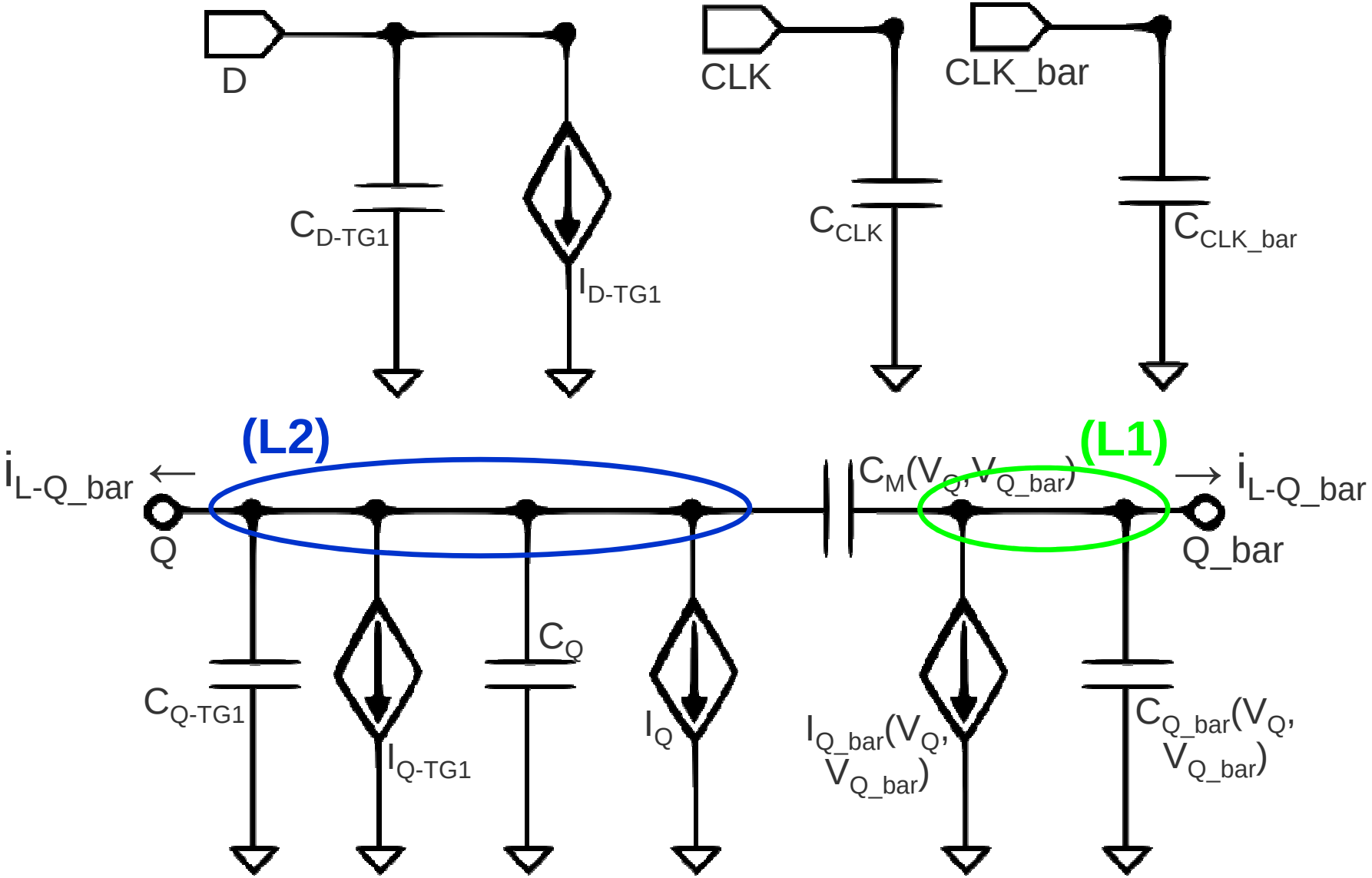
$$(\mathrm{I1})\; i_o + I_o(V_i, V_o) + \left(C_o(V_i, V_o) + C_M(V_i, V_o)\right)\frac{dV_o}{dt} - C_M(V_i, V_o)\frac{dV_i}{dt} = 0$$

- All parameters determined as a function of V_o and V_i
- Arbitrary load connected to V_o
- i_o is a function of V_o and the load
- Connect arbitrary input voltage to V_i

→ solve differential equation to determine V_o (Euler)

Characterization of the CSM for the latch

- Start by characterizing TG1
- Attach voltage sources to Q, Q_bar, CLK and CLK_bar
- Step by step all capacitances and currents in the 3 modes are characterized


D
CLK
CLK_bar
$C_{D\text{-}TG1}$
$I_{D\text{-}TG1}$
C_{CLK}
C_{CLK_bar}
(L2)
(L1)
$i_{L\text{-}Q\_bar}$
Q
$C_M(V_Q, V_{Q\_bar})$
$i_{L\text{-}Q\_bar}$
Q_bar
$C_{Q\text{-}TG1}$
$I_{Q\text{-}TG1}$
C_Q
I_Q
$I_{Q\_bar}(V_Q, V_{Q\_bar})$
$C_{Q\_bar}(V_Q, V_{Q\_bar})$

Output Calculation (Complete Latch)

(L1)

$$i_{L-Q\_bar} + I_{Q\_bar}(V_Q, V_{Q\_bar}) - C_M(V_Q, V_{Q\_bar})\frac{dV_Q}{dt} + \left[C_M(V_Q, V_{Q\_bar}) + C_{Q\_bar}(V_Q, V_{Q\_bar})\right]\frac{dV_{Q\_bar}}{dt} = 0$$

(L2)

$$i_{L-Q} + I_Q + I_{Q-TG1} - C_M(V_Q, V_{Q\_bar})\frac{dV_{Q\_bar}}{dt} + \left[C_M(V_Q, V_{Q\_bar}) + C_Q + C_{Q-TG1}\right]\frac{dV_Q}{dt} = 0$$

- All parameters determined as a function of V_Q and V_{Q_bar}
- Arbitrary load connected to Q and/or Q_bar
- $i_{L\text{-}Q\_bar}$ / $i_{L\text{-}Q}$ is a function of the two voltages and the load
- Connect arbitrary input voltage to D (effects $I_{Q\text{-}TG1}$ and $C_{Q\text{-}TG1}$)

→ solve differential equation to determine V_Q and V_{Q_bar} (Euler)