Principles of Current Source Modeling

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Outline

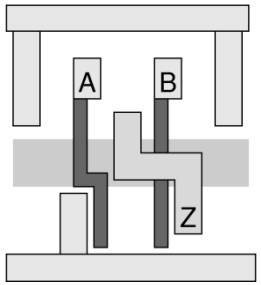
- Brief Introduction
- Evolution of Timing Models
- Current Source Models
  - Basics
  - Characterization
  - Implementation
  - Application
- Summary

Current Source Models in a Nutshell

- Highly accurate timing models for DSM designs
- CSMs are transistor models for logic gates.
- A holistic model for timing, noise, and power analysis.
- Means to reduce SPICE simulation times.

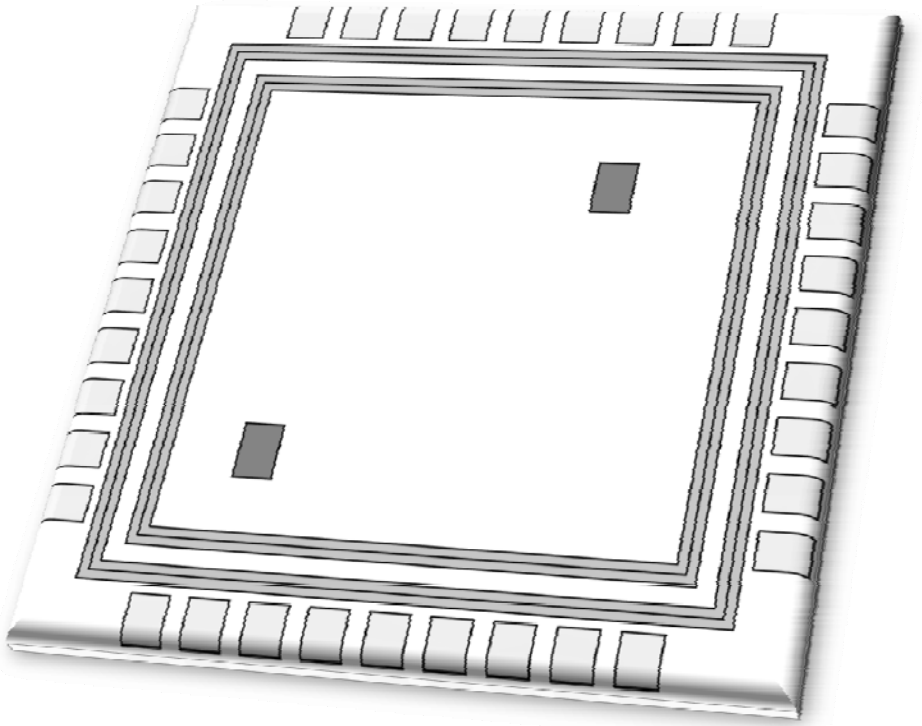
Optimization for Timing, Area, Power, and Yield

```
MODULE CHIP (...)
 NAND(Z1, in2, in1);
 NAND(Z2, A, Z1);
  ...
ENDMODULE
```

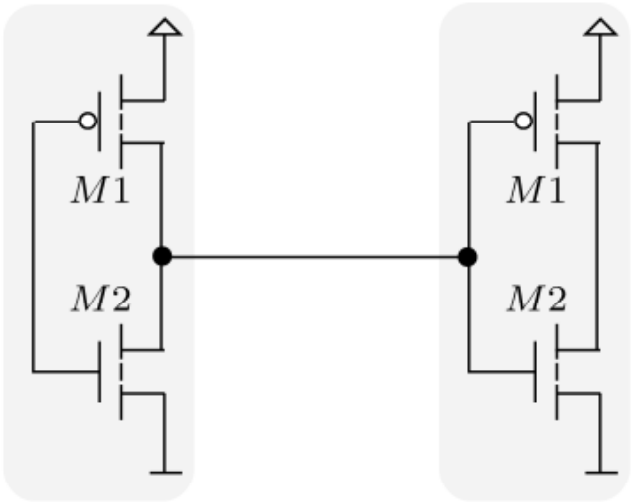


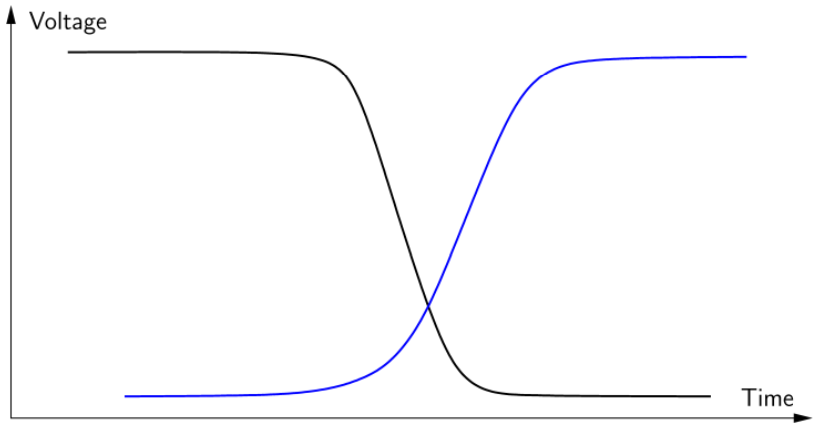
Abstract views of standard cells

Area, Power, and Timing



Simple Approach to Cell Delay





Fixed (maximum) value for all gate.
Fixed (maximum) value for each gate

Overview on Delay and Waveform Models (1)

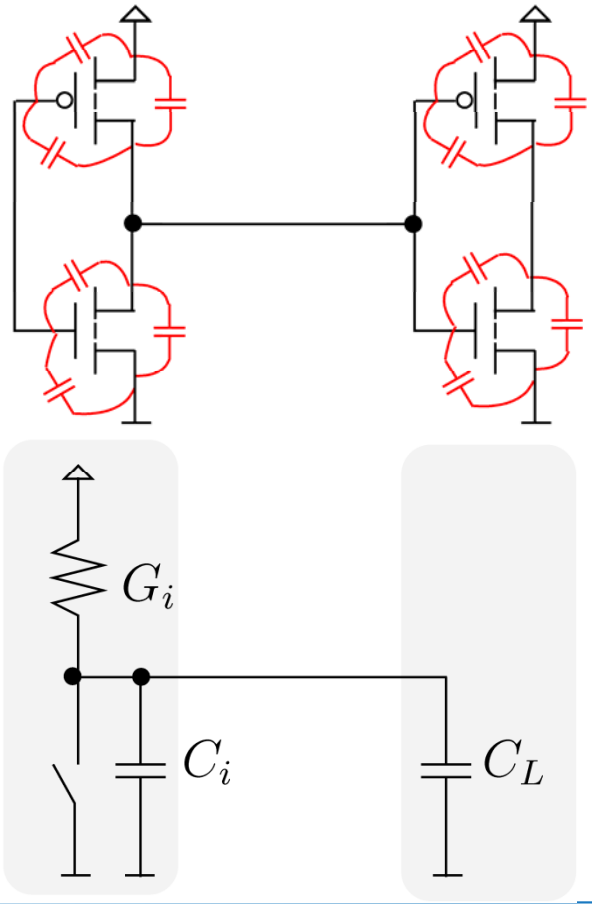
gate delay

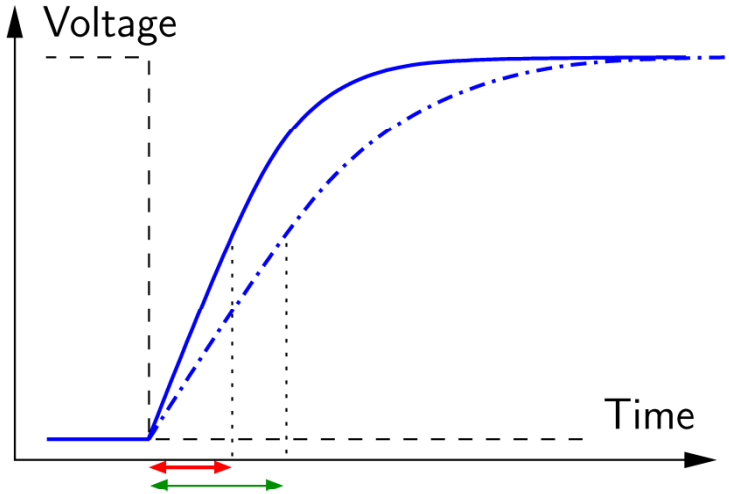
$d = const$

t_{arr}

signal model

Helmholtz-Thévenin Model for Cell Delay

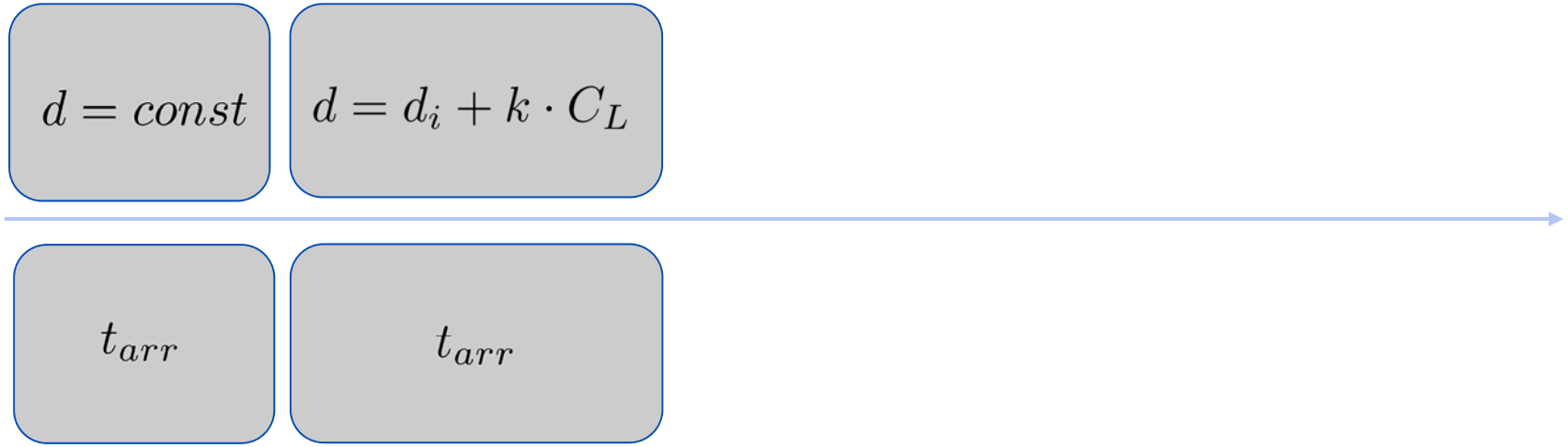




$$d = d_i + k \cdot C_L$$

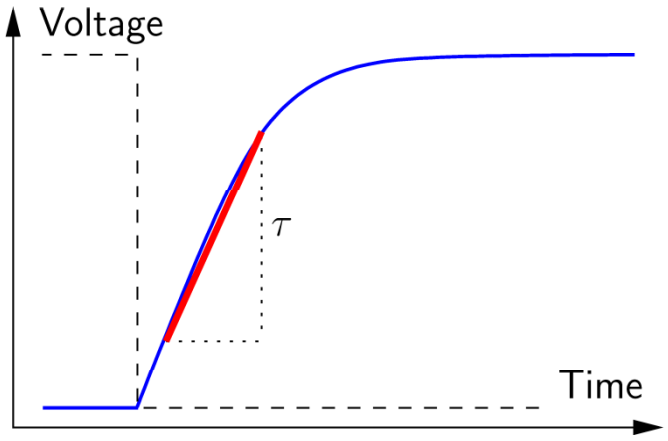
Overview on Delay and Waveform Models (2)

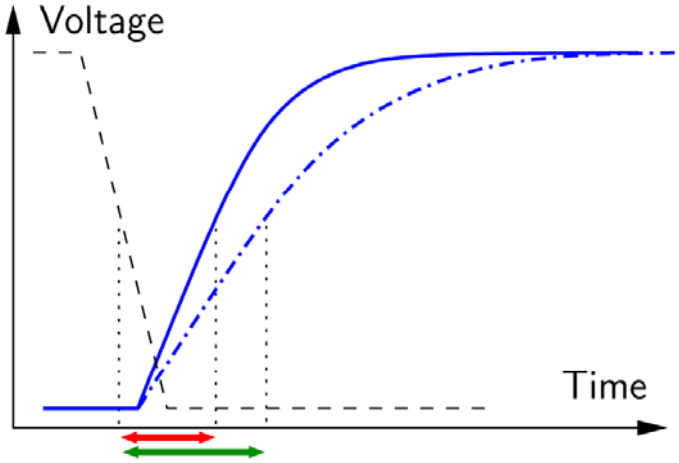
gate delay

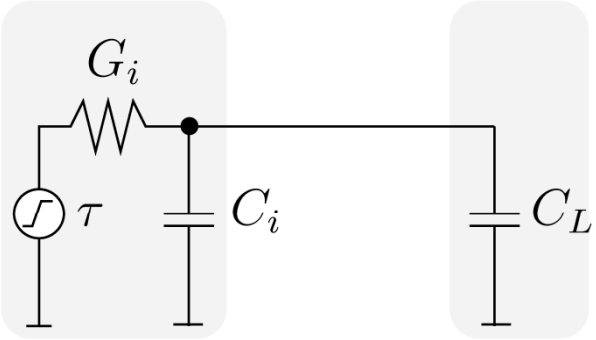


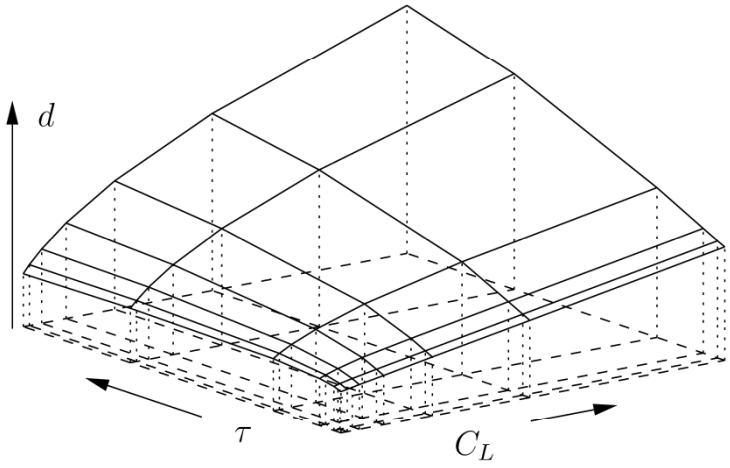
signal model

Nonlinear Delay Model - NLDM



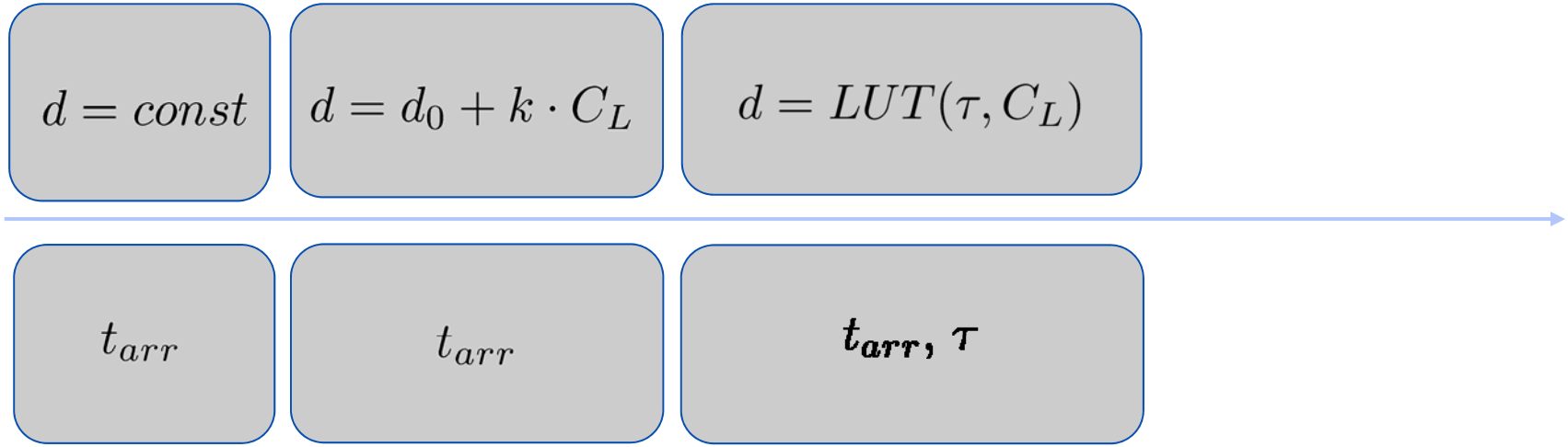






Overview on Delay and Waveform Models (3)

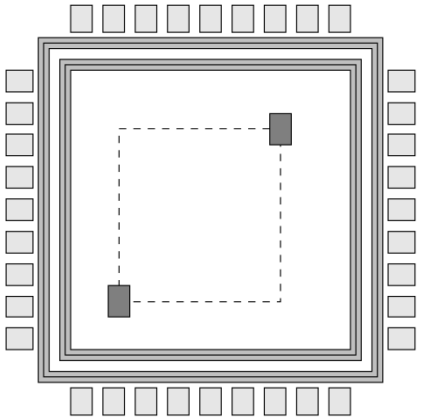
gate delay

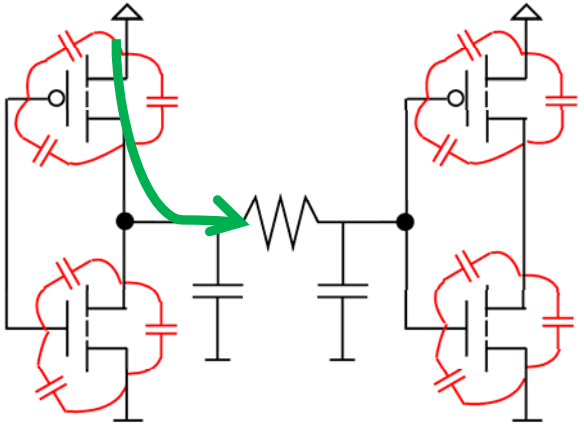


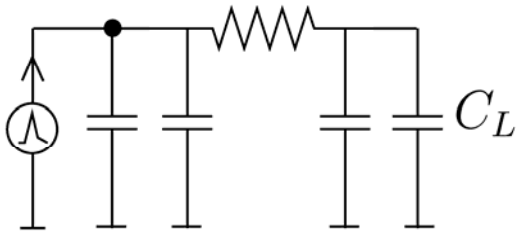
signal model

t_{arr}, τ, LUT : Arrival time, signal slope, lookup table

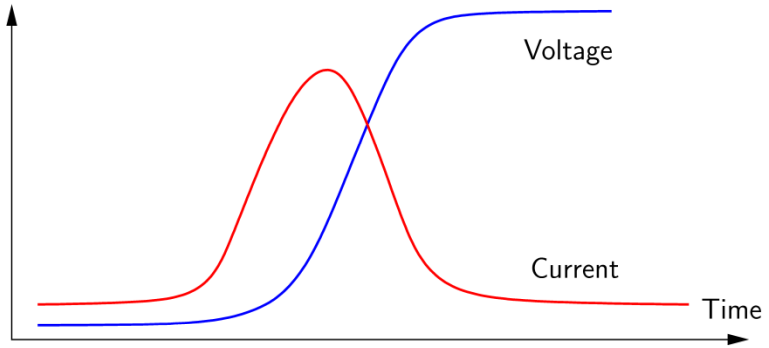
RC Interconnect and the Analog side of Logic Cells





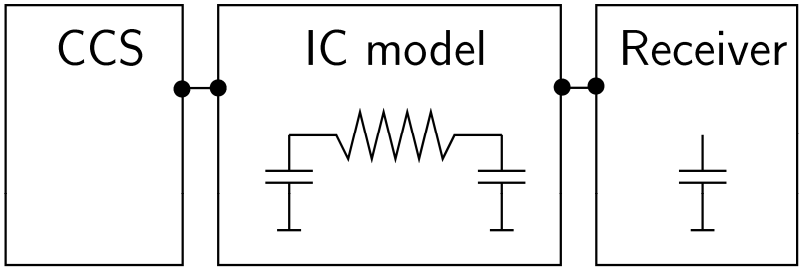


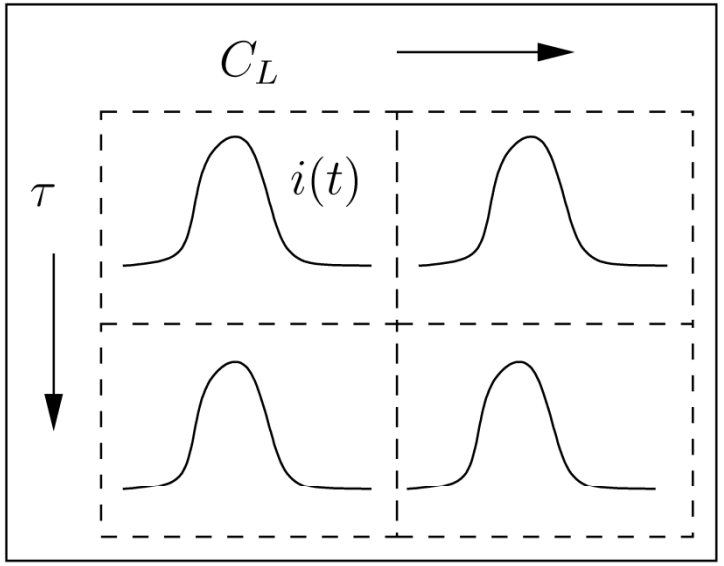
Transistors are voltage controlled current sources.



Composite Current Source Model - CCS

- Replacement/Adhencement for NLDM
- Highly resistive interconnects



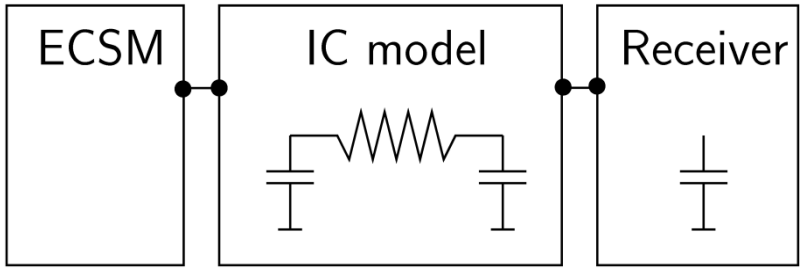


$$\begin{matrix}[t_1, & t_2, & t_3, & \ldots] \\ [i(t_1), & i(t_2), & i(t_3), & \ldots]\end{matrix}$$

$$v(t_{n+1}) = v(t_n) + \frac{1}{C_{eff}} \int_{t_n}^{t_{n+1}} i_{avg} dt$$

Effective Current Source Model - ECSM

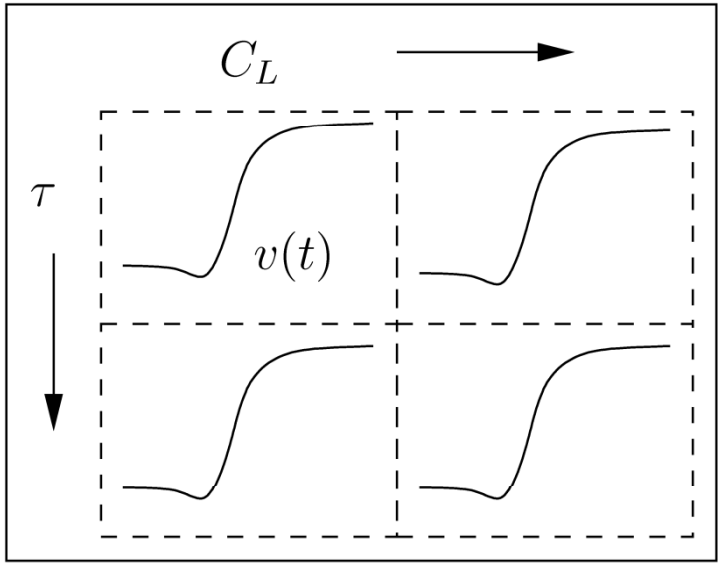
- Additionally voltage waveform



$$\begin{matrix}[t_1, & t_2, & t_3, & \ldots] \\ [v(t_1), & v(t_2), & v(t_3), & \ldots]\end{matrix}$$

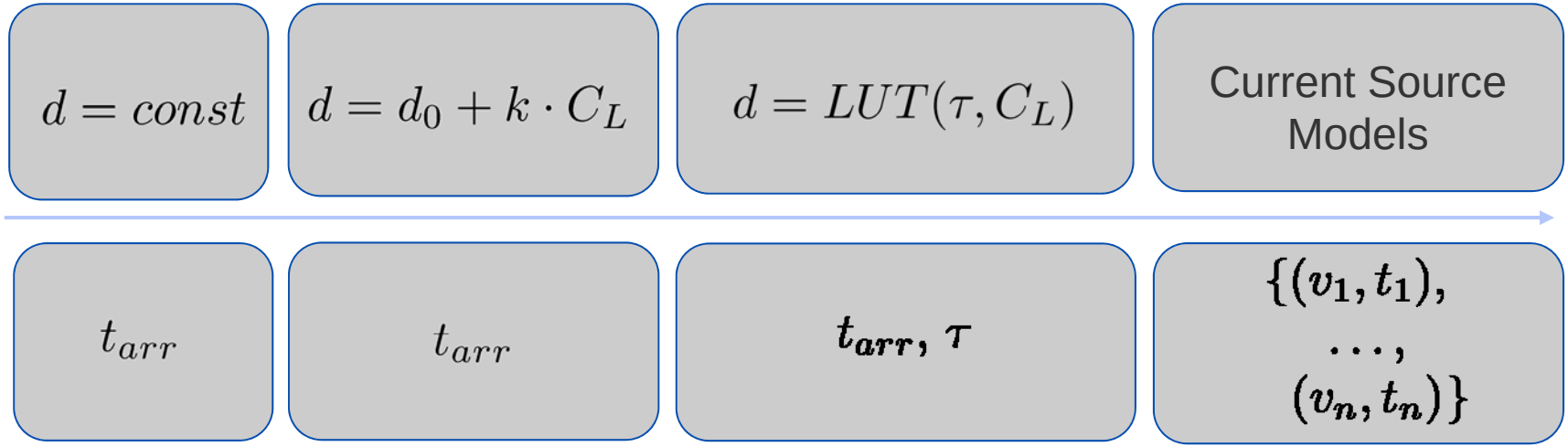
$$C_{load}$$

$$i = C_{load}\frac{dV}{dt}$$
$$v_(t_{n+1}) = v(t_n) + \frac{1}{C_{eff}}\int_{t_n}^{t_{n+1}} idt$$



Overview on Delay and Waveform Models (2)

gate delay



signal model

t_{arr}, τ, LUT : Arrival time, signal slope, lookup table

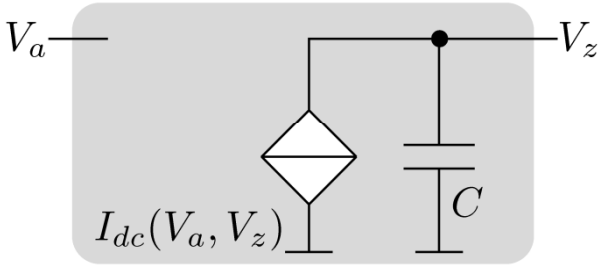
Waveform Independent Delay Models - CSM

- Model port currents as functions of port voltages
- At least one voltage controlled current source
- Additional components to model dynamic behaviour
  - Capacitors
  - Delay lines
  - Charges
  - Filters
- Usually one CSM per timing arc

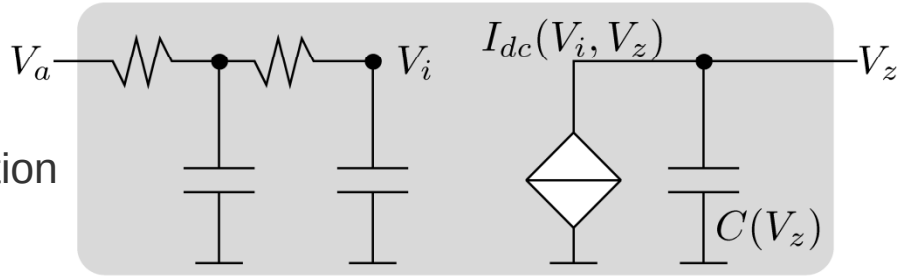
$$\hat{I}_{port} = f(V_{in}, V_{out})$$

Different CSM approaches

- Blade and Razor [Croix03]
  - shape of output waveform
  - Delay added
  - Error minimization

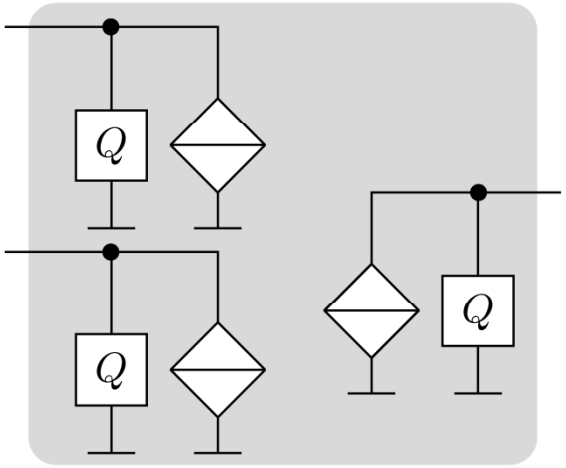


- CSM of Peng Li et. al.
  - SPICE compatible
  - Model parameters by error minimization
  - Tuning of parameters

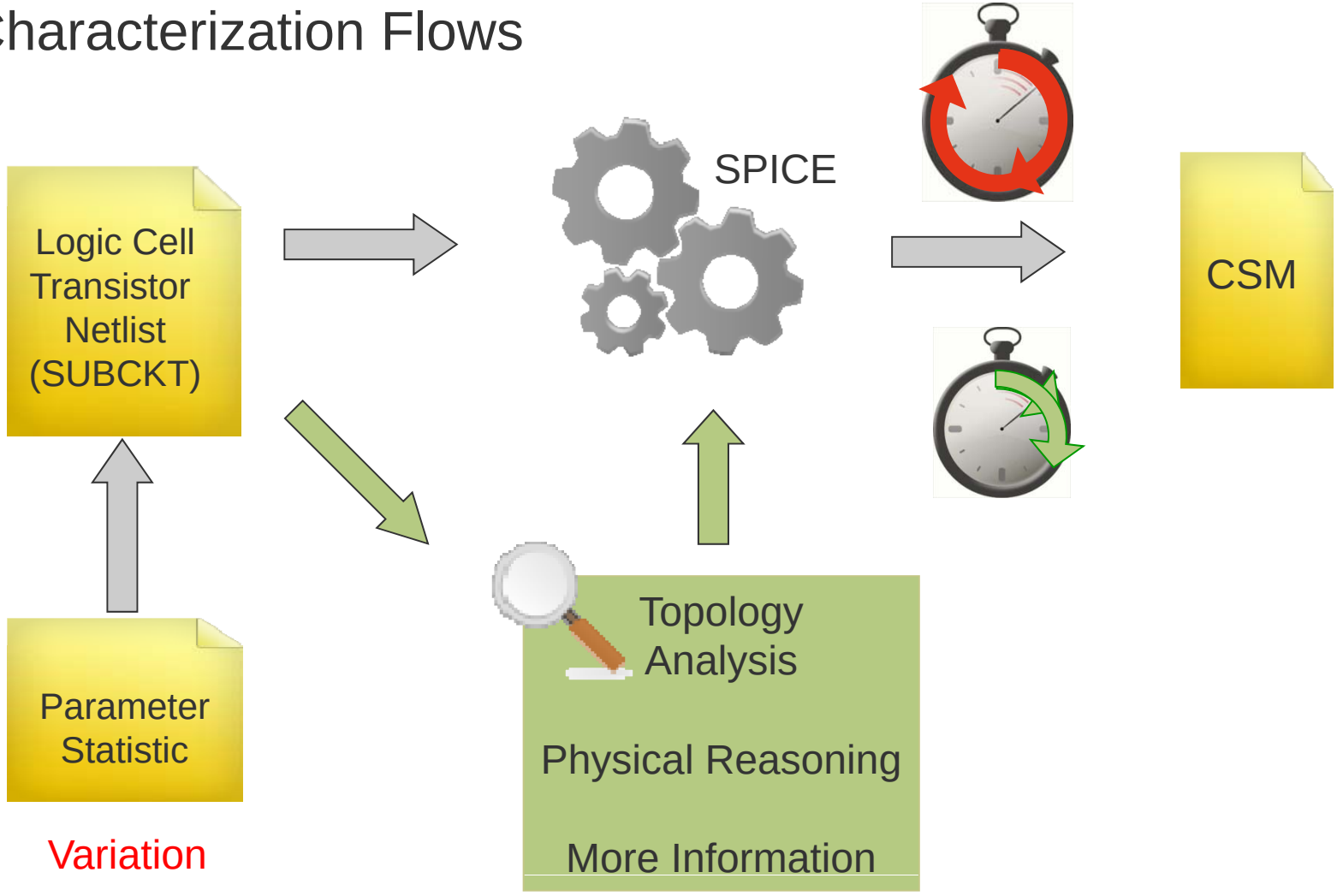


Different CSM approaches

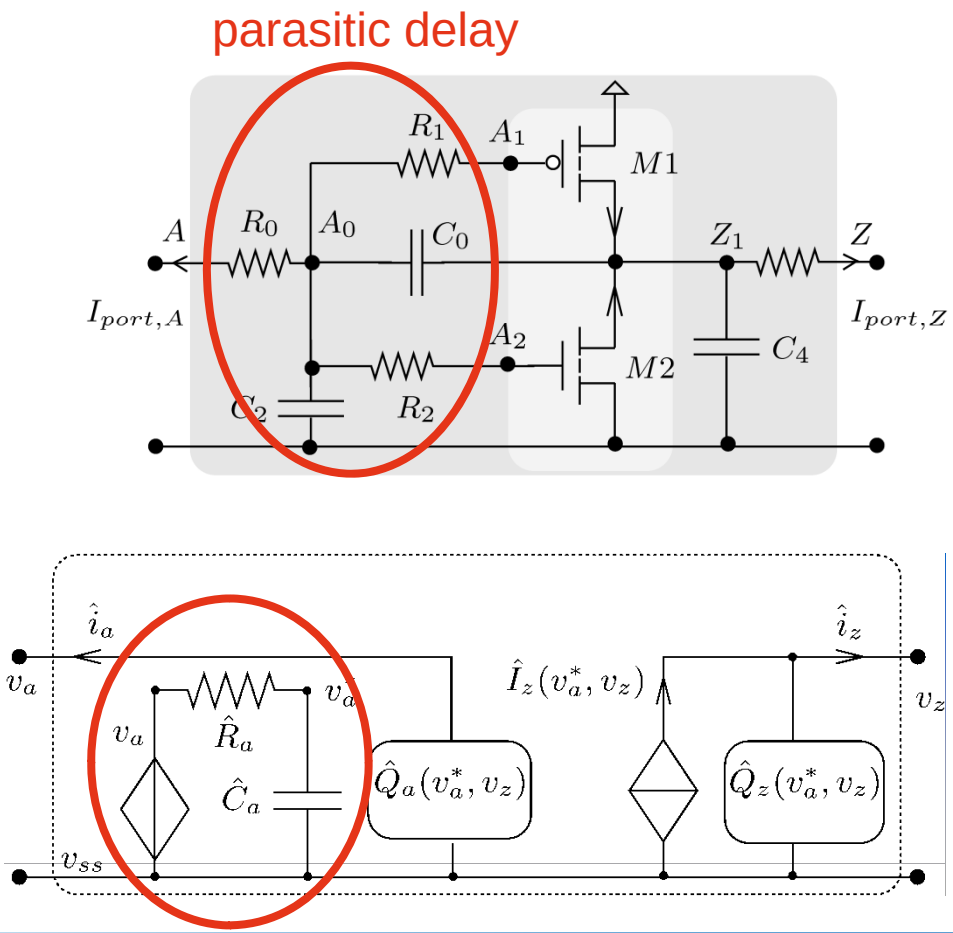
- General Model [Amin06]
  - Current and charges are functions of all port voltages
  - Multiple input switching
  - Internal nodes



Characterization Flows



Relation between Logic Cell and Current Source Model



CSM

- DC port currents
- port charges
- lowpass filter
  (only for large gates)

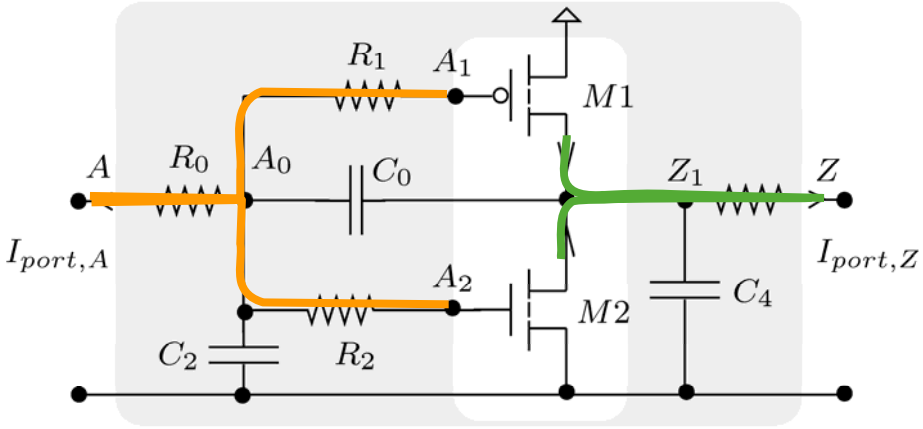
$$i(\mathbf{v}, \dot{\mathbf{v}}(t)) = \hat{i}(\mathbf{v}, \dot{\mathbf{v}}(t))$$

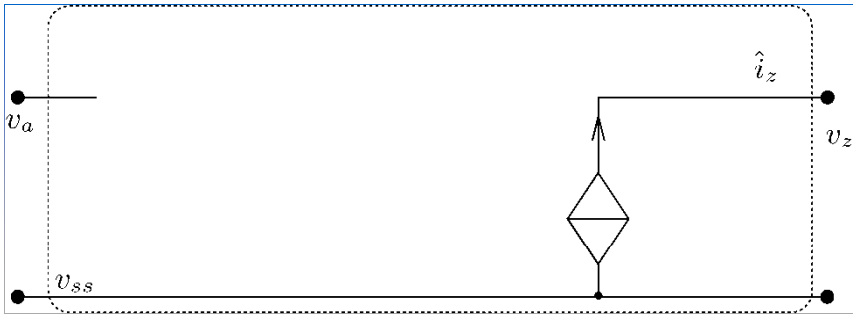
$$\hat{I}_{z,1} = f(v_a^*, v_z)$$

$$\hat{Q}_a = g(v_a^*, v_z),\ \hat{I}_{dyn,a} = \dot{\hat{Q}}_a$$

$$\hat{Q}_z = h(v_a^*, v_z),\ \hat{I}_{dyn,z} = \dot{\hat{Q}}_z$$

DC-Transfer Characteristic





$$\hat{I}(\mathbf{v}, 0) = I_{cir}$$

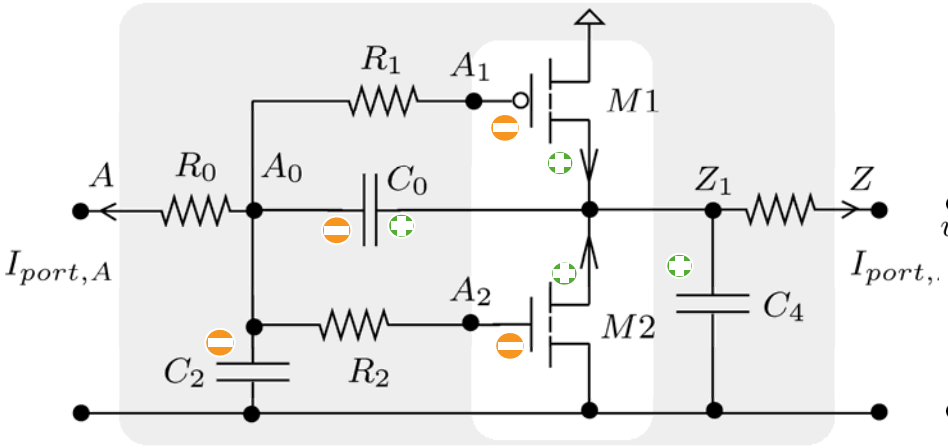
$$I_A = I_{g,M1} + I_{g,M2} \approx 0$$

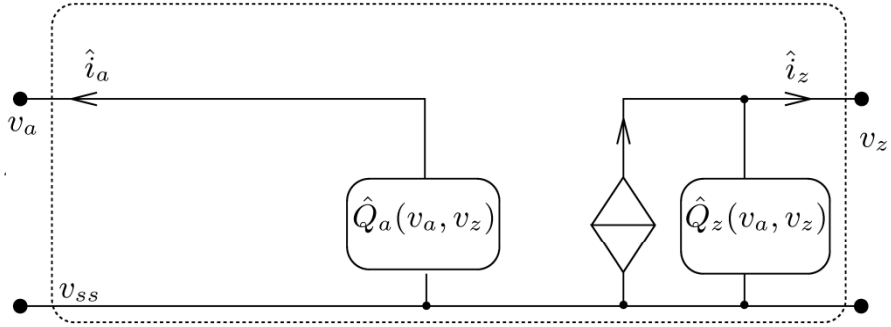
$$I_Z = I_{d,M1} + I_{d,M2}$$

Automaticaly derived from netlist

DC simulation

Additional Dynamic Port Current





$$i_{cir}(\mathbf{v}, \dot{\mathbf{v}}) = \hat{i}(\mathbf{v}, \dot{\mathbf{v}}) = \hat{i}(\mathbf{v}) + \dot{\hat{Q}}(\mathbf{v})$$

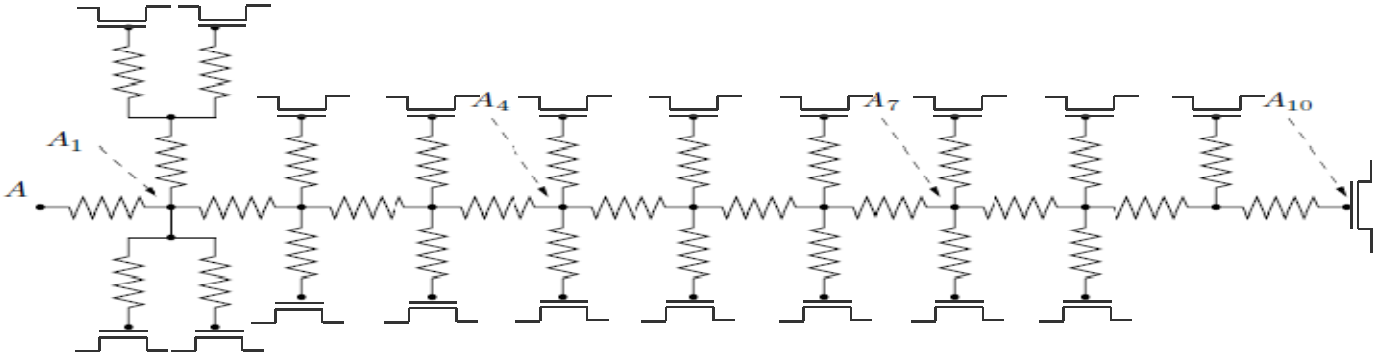
$$Q_A = Q_{g,M1} + Q_{g,M2} + Q_{C_2,A_0} + Q_{C_0,A_0}$$

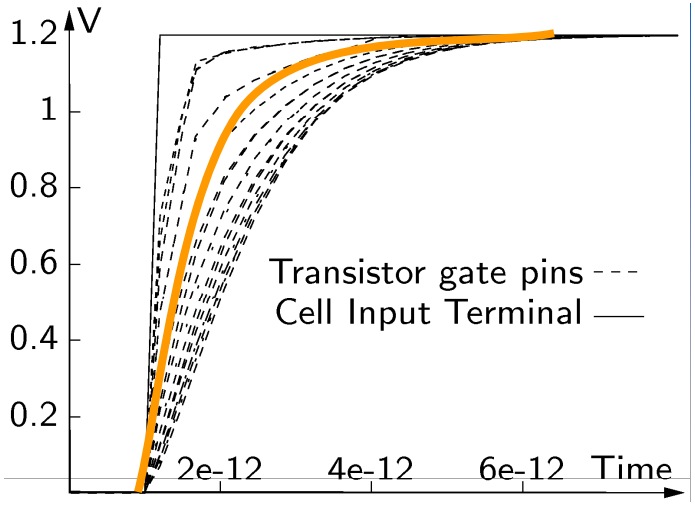
$$Q_Z = Q_{d,M1} + Q_{d,M2} + Q_{C_1,Z_1} + Q_{C_0,Z_1}$$

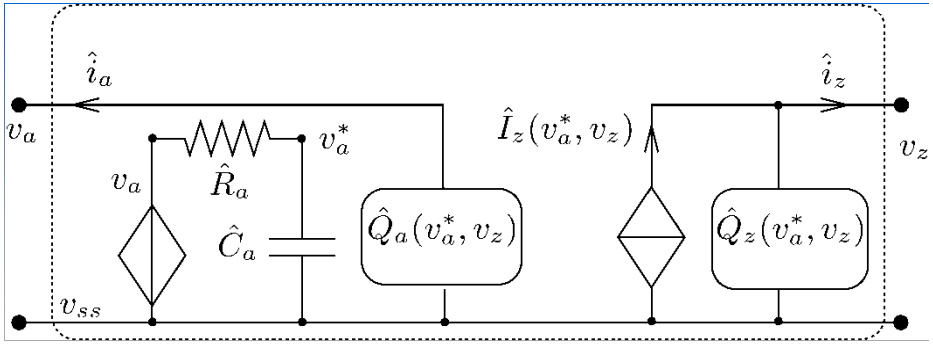
Automatically derived from netlist

DC simulation

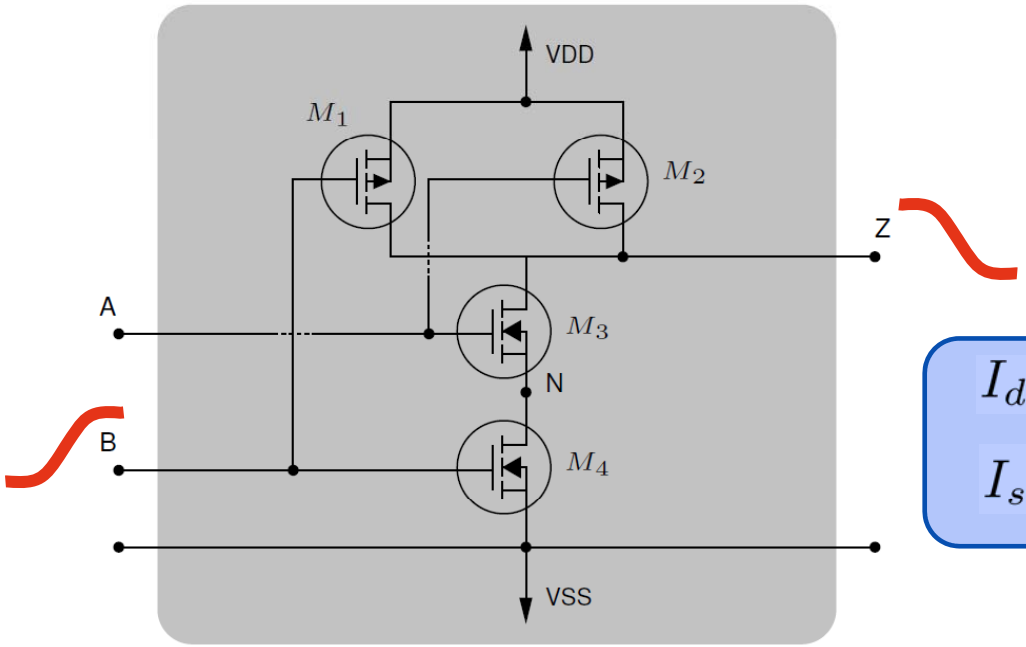
Voltage Approximation Error for Large Inverter (input)







Characterization - cells with stacked transistors



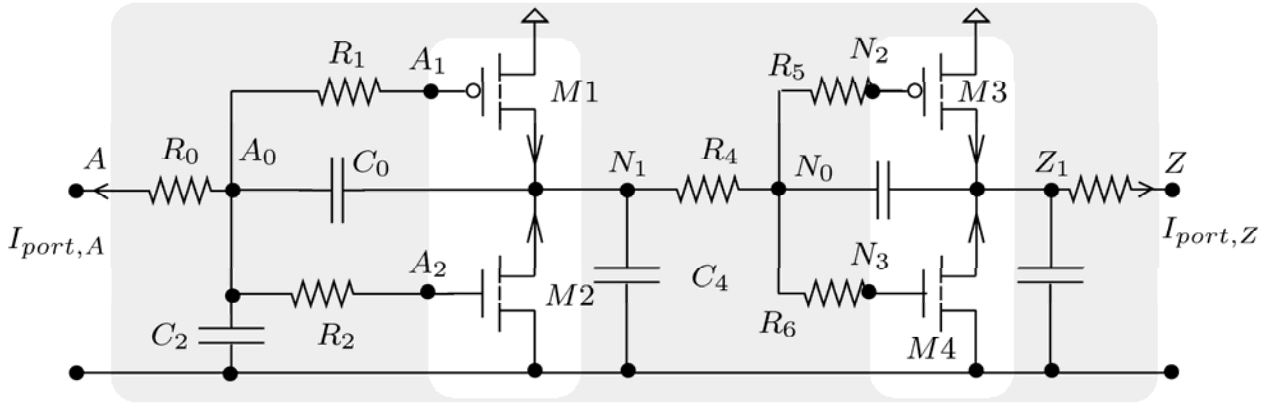
$$I_{d,M3} = -I_{s,M3}$$

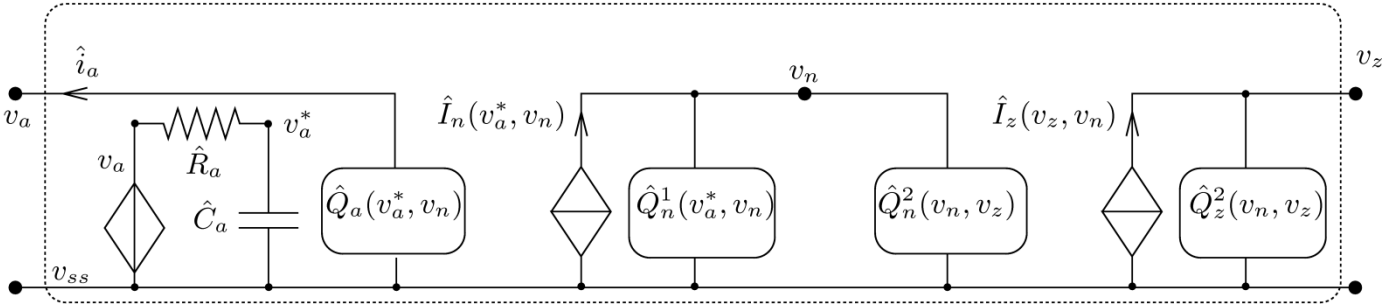
$$I_{s,M3} = -I_{d,M4} + \dot{Q}_{s,M3} + \dot{Q}_{d,M4}$$

$$I_{\text{out}} = I_{d,M1} + I_{d,M2} + I_{d,M4}$$

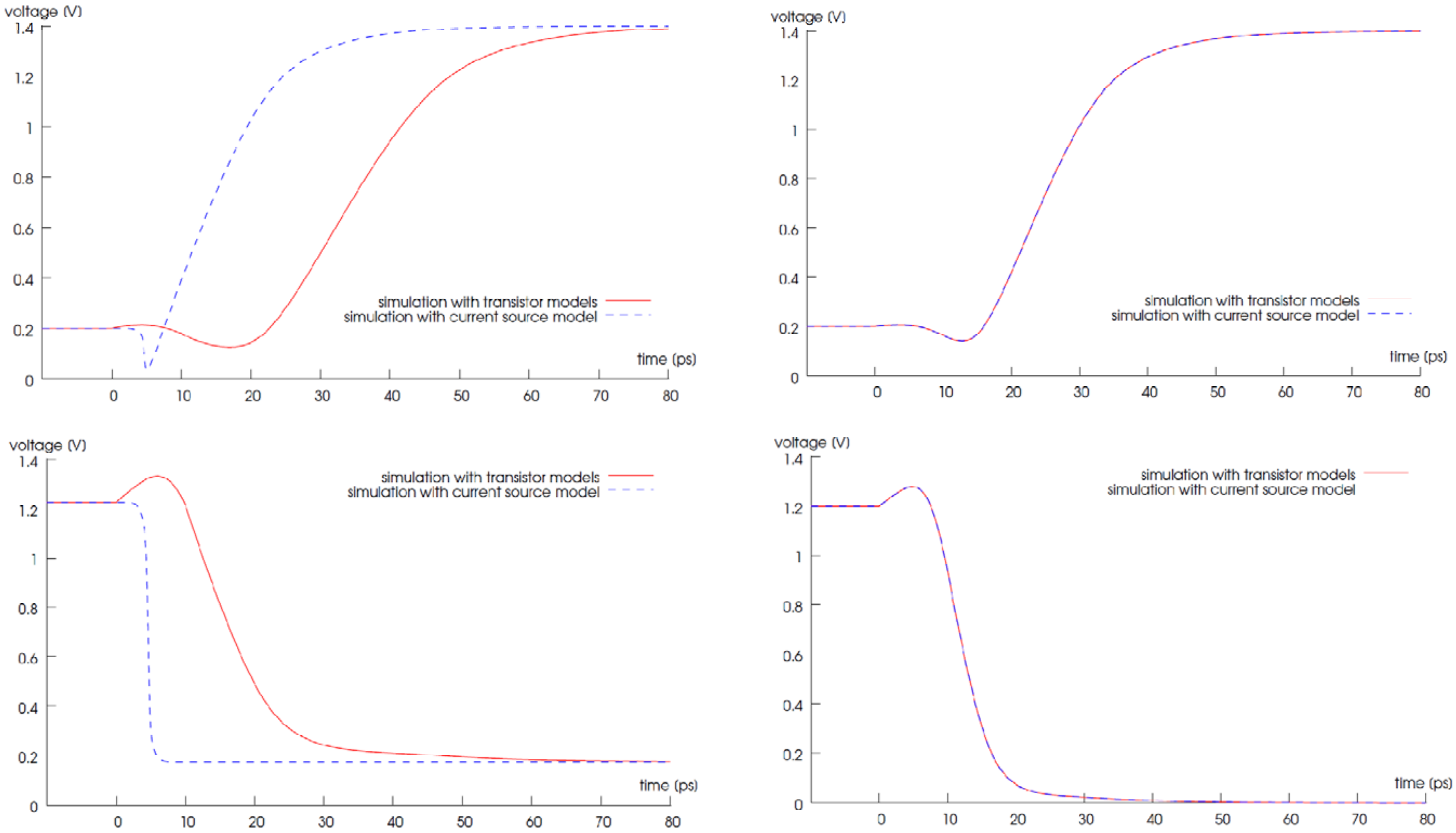
$$Q_{\text{out}} = Q_{d,M1} + Q_{d,M2} + Q_{d,M3} + Q_{s,M3} + Q_{d,M4}$$

Model each Channel Connected Block

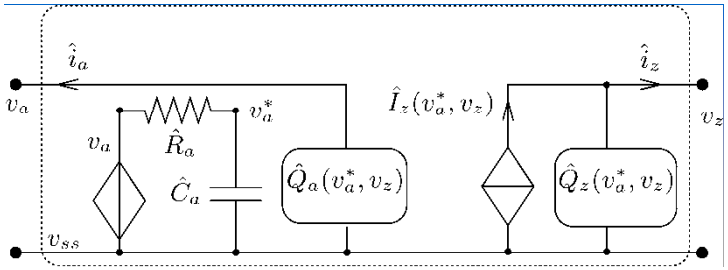


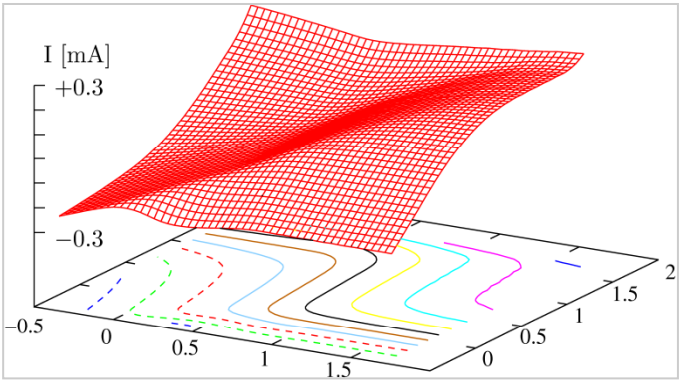


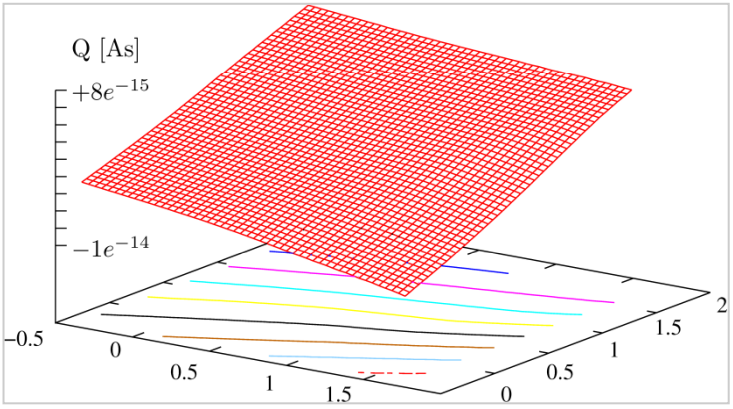
Simulation for Buffer gate (parasitic layout)

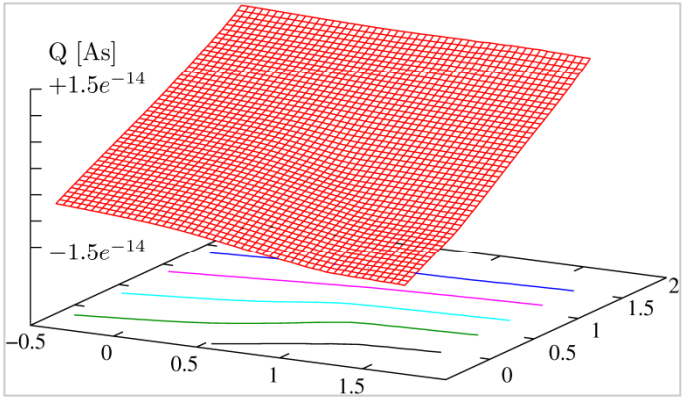


Typical Lookup Tables for Model Components





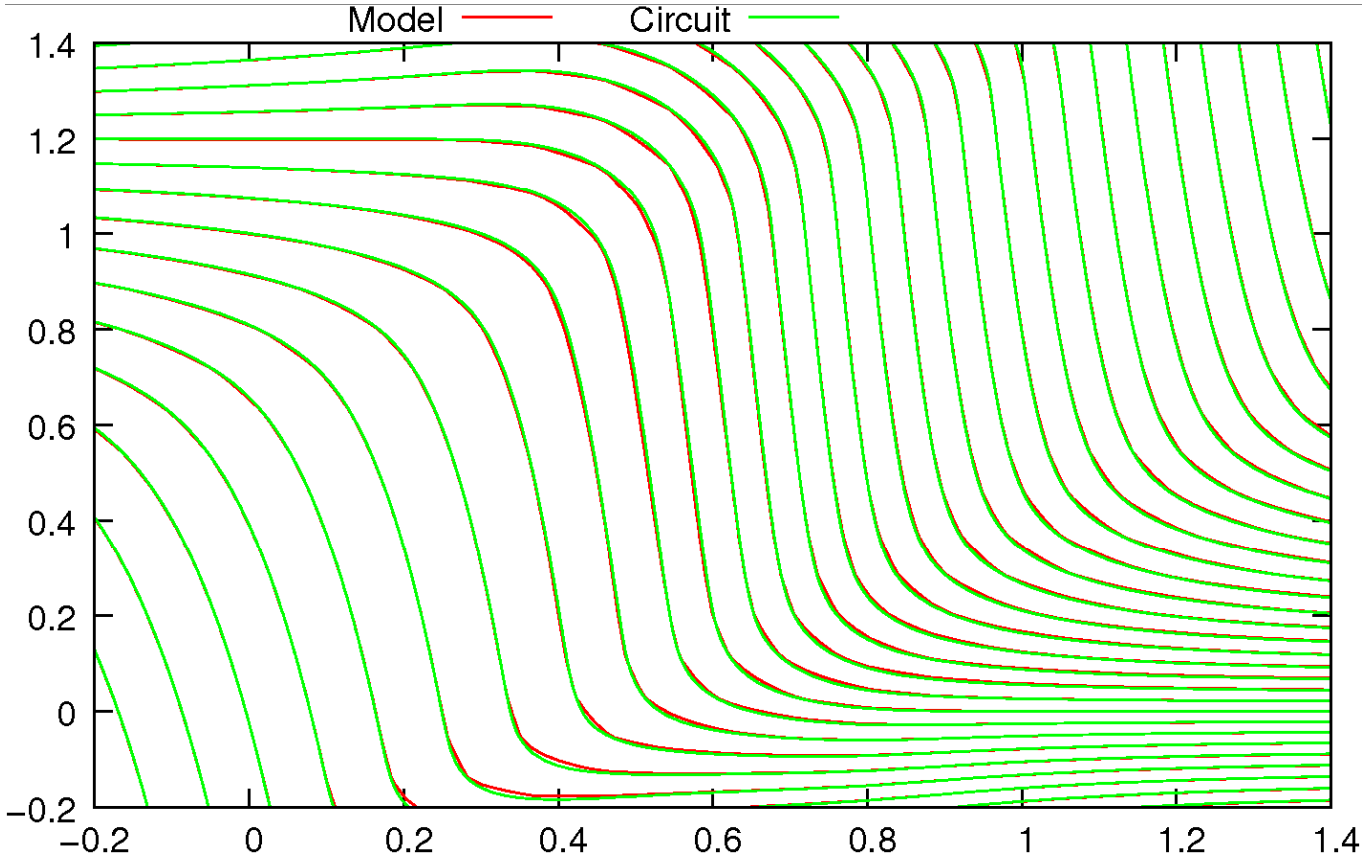




Approximation of Lookup Tables

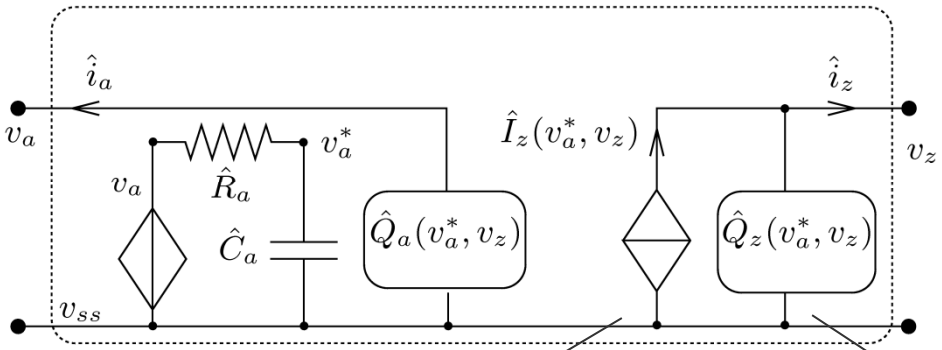
- Radial Base Functions [1]
- Splines
- Legendre Polynoms [Goel08]

Comparison of Static Output Current



bilinear Interpolation, 50x50 grid, 100x100 for simulation

Model Implementation




```
.SUBCKT R_SND3X015_A11_Z A B C Z VDD VSS

ZCHR_IN_A_Z A VSS Z VSS Z_CHARGE
+ params=(D_XL_THIN=XL_THIN D_XW_THIN=XW_THIN D_NDEP_NREG=NDEP_NREG)
+ MODLIB='CSM2'
+ file='R_SND3X015/ZMS/R_SND3X015_Q_A_Z_A10_Z01_B1_C1'

ZCUR_OUT_Z_A Z VSS A VSS Z_CURRENT
+ params=(D_XL_THIN=XL_THIN D_XW_THIN=XW_THIN D_NDEP_NREG=NDEP_NREG)
+ MODLIB='CSM2'
+ file='R_SND3X015/ZMS/R_SND3X015_I_Z_A_A10_Z01_B1_C1'

ZCHR_OUT_Z_A Z VSS A VSS Z_CHARGE
+ params=(D_XL_THIN=XL_THIN D_XW_THIN=XW_THIN D_NDEP_NREG=NDEP_NREG)
+ MODLIB='CSM2'
+ file='R_SND3X015/ZMS/R_SND3X015_Q_Z_A_A10_Z01_B1_C1'

.ENDS
```

VCCS:
Compiled Models (C-Code)
$tablemodel (Verilog-A)

VC dynamic CS:
C (constant capacitor)
C(v) (voltage controlled capacitor)
Compiled Models (C-Code)
$tablemodel (Verilog-A)

- Data needed during Initialization
- Calculations during Newton Iteration
- Memory footprint (50x50, at least 3 tables)

CSM Implementation for SPICE Simulators

```
.SUBCKT R_SND3X015_A11_Z A B C Z VDD VSS

ZCHR_IN_A_Z A VSS Z VSS Z_CHARGE
+ MODLIB='CSM'
+ file='R_SND3X015/ZMS/R_SND3X015_Q_A_Z_A10_Z01_B1_C1'

ZCUR_OUT_Z_A Z VSS A VSS Z_CURRENT
+ MODLIB='CSM'
+ file='R_SND3X015/ZMS/R_SND3X015_I_Z_A_A10_Z01_B1_C1'

ZCHR_OUT_Z_A Z VSS A VSS Z_CHARGE
+ MODLIB='CSM'
+ file='R_SND3X015/ZMS/R_SND3X015_Q_Z_A_A10_Z01_B1_C1'

.ENDS
```

Our experience

- Bilinear Interpolation is fine
  - Bottleneck is Model-Simulator-Communication
- Nonlinear Charges
  - also bilinear interpolation
  - many might look good but others are nonlinear
  - Derivativ matters!
- Best suited to long resistive interconnects
  - This is very other models fail
- Dimensions
  - Memory expensive 3D tables
- Speed
  - 50 – 200X w.r.t. modern SPICE simulators
  - 5-10X w.r.t. FastSPICE simulators

Summary on Current Source Models

- Very accurate delay models for logic cells
- Arbitrary loads and waveform -> SI, Timing, Noise
- In SPICE Simulators or special purpose simulators
- Naming ambiguity with EDA vendors

Thank you for your attention